Self-Packaged Miniature Microwave Filters based on Multilayer Liquid Crystal Polymer Technology

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Abstract

The following thesis is concerned with the development of fabrication techniques and novel designs for self-packaged, multilayer circuits using liquid crystal polymer (LCP) materials exclusively, given the favourable characteristics this material has for microwave circuits.

Fabrication techniques are aimed at the production of miniature, low-profile filters. Advanced techniques for production of interlayer via connections are investigated and new methods proposed, with special attention at the lamination process and production of vertical, inter-layer transitions. Results obtained demonstrate the fabrication process is reliable for producing multilayer filters, with up to four metal layers, and via transitions in the region of 0.2 mm diameter.

The fabrication process has been developed during this work is applied to novel filter designs, covering dual-band filters and lowpass filters. A new structure for dual-band filter is proposed, using folded multimode resonators (FMSIR). This structure is validated through the fabrication of two different filters with passbands 1.2/2.4 GHz, and 2.4/5 GHz, showing deep off-band rejection.

Low pass structure covered in this thesis is based on the principle of destructive interference and aims at low insertion loss and out-of-band rejection higher than 40 dB. Fabricated samples validate the design showing a rejection in the region of 42 dB, with a cutoff frequency of 3 GHz. Its small footprint and low insertion loss allows this type of filters to be used as cleanup filters. All the designs covered in this work are simulated using CAD tools and then validated by measurements on fabricated samples.

Dedication

To my family, specially to those who left us.

Also to Renate for putting up with me all this time.

Acknowledgements

I would like to thank my supervisor Professor Jiasheng Hong for his support and guidance throughout my study period at Heriot Watt University, as well as my industrial supervisor Dr. Neil Thomson. Without their support and encouragement this work would have not been possible.

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[J1] F. J. Cervera, and Jiasheng Hong, "High rejection, Self-packaged Lowpass Filter using Multilayer Liquid Crystal Polymer Technology", *IEEE Trans. Microw. Theory Techn.* Vol. 63, No. 12, pp.3920-3928, Dec 2015

[J2] F. J. Cervera, and Jiasheng Hong, "Compact Self-Packaged Dual-Band Filter Using Multilayer Liquid Crystal Polymer Technology", *IEEE Trans. Microw. Theory Techn.* Vol. 62, No. 11, pp.2618-2625, Nov 2014

Conferences

[C1] F. J. Cervera, and Jiasheng Hong, and Neil Thomson "Development of packaged UWB passive devices using LCP multilayer circuit technology", *42nd European Microwave Conference (EuMC), 2012* pp.1150-1153, Oct 2012

[C2] Jiasheng Hong, and F. J. Cervera "Recent development of compact microwave filtering structures based on multilayer LCP technology", *Asia-Pacific Microwave Conference Proceedings (APMC), 2012* pp.779-781, Dec 2012

Chapter 1

Introduction

From mobile communications to radar or medical field, wireless systems and applications have become indispensable in our daily lives. As the number of solutions increases, the demand for frequency allocation also grows, making the radiofrequency (RF) spectrum more crowded. Hence, the frequency spacing between bands smaller and even some of the bands overlap each other, as it is the case of ultra-wide band (UWB) (3.1 - 10.6 GHz) and wireless local access network (5 - 6 GHz). Therefore, improved filtering devices are required to meet the challenges that such a crowded RF spectrum presents. Moreover, new filters also have to meet the requirements of small size and light weight, not to mention low cost. In order to achieve this, new materials and fabrication techniques have been investigated lately.

In recent years two types of materials are attracting much of the attention of the RF community: low temperature co-fired ceramic (LTCC) and liquid crystal polymer (LCP). Both materials offer good electrical properties to be used as circuit substrate. However, LCP has the advantage, among others, of requiring much lower temperature for manufacturing, along with lower price.

LCP is a relatively new plastic material that shows many characteristics that make it a good candidate to address the mentioned challenges. On the electrical side, its low permittivity and loss tangent, stable from low frequency up to frequencies above 100 GHz, make LCP a potentially good substrate for microwave applications. Furthermore, on the mechanical side, apart from its very light weight, LCP shows low moisture absorption and high temperature capability, leading to high stability across different environmental conditions.

Despite the favourable conditions of LCP for microwave applications, such as filters and antennas, the manufacturing processes and techniques involved are still in development and there are several challenges that need to be addressed.

RF and millimetre systems will often have to work in hostile conditions of temperature and humidity, hence the need for a package that protects the system from the environment. Given the mechanical properties of LCP, investigations on using LCP not only as a substrate, but also as a packaging material have been carried lately.

The main use of LCP is the fabrication of multilayer, planar filters. LCP is available in very thin films, enabling strong coupling between adjacent metal layers and leading to novel designs in areas such as bandpass or lowpass filters.

1.1 Objectives

Owing to its title, this thesis aims at developing self-packaged, multilayer filters using LCP as substrate. Initial requirements for these filters are a very low insertion loss combined with a type of package that would allow for easy interconnection in a host system. It was also a main interest applying this requirements to a low-pass filter with a wide, deep rejection, as covered in Chapter 5. Additionally, a band-pass filter was to be investigated, aiming at a reduced footprint compared to the work found in the open literature.

Successfully achieving this aim requires dividing the task into three different interconnected sections (Fig. 1.1):

- Development of multilayer LCP fabrication techniques
- Development of a packaging solution
- Multilayer filter design

Multilayer LCP fabrication techniques is an active field of research, even though the process is still in development. In [1], LCP properties are extensively covered, along with fabrication techniques. However, described techniques are mainly focused on the development of packages, rather than multilayer circuits. Given the lack of information, one of the main focuses of this project is the development of an in-house fabrication process, addressing problems like the number of layers used and

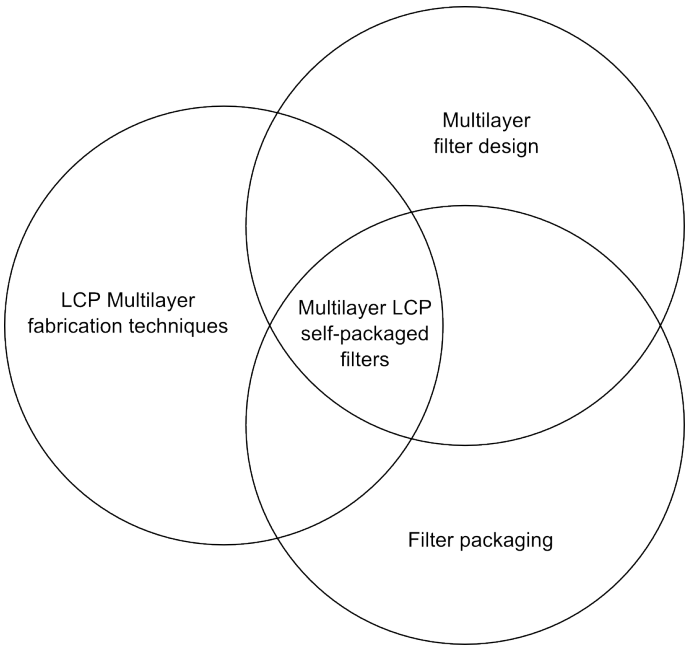

Figure 1.1: Project objectives

the production of reliable interlayer connections.

Another concern of this thesis is the packaging. Usually the packaging is an external solution added to the already designed filter. The aim is to integrate the packaging in the design stage, so the package is flexible to adapt to the filter, allowing for both to be fabricated in the same process. As such, the first stage would be to design broadband vertical launches working up to 20 GHz and a process for manufacturing the LCP substrate into a hermetic surface mount package, with careful attention to production issues.

Parallel to the development of fabrication techniques and packaging, different topologies for multilayer filters are investigated and integrated with the proposed packaging. Initially these filters are developed as stripline and once the design is complete, they are integrated in the proposed packaging solution.

1.2 Overview

In order to cover the topics set as aim, this thesis is organised as follows:

Chapter 2 covers the development of the fabrication process, starting from the in-house fabrication process available at the beginning of the project. It is described and its weak points highlighted. Some ideas are proposed towards improvement of

the process, ending with an optimized fabrication process.

In Chapter 3 the need for packaged filters is discussed. A review of solutions traditionally used is covered, followed by the proposed method for producing self-packaged filters. Several designs are introduced, comparing its performances both in terms of electromagnetic losses and fabrication issues.

The following two chapters apply the methods discussed for fabrication and self-packaging towards multilayer filter design of a dual-band filter, in Chapter 4, and a lowpass in Chapter 5. The proposed dual-band filtering structured is based on a pair of coupled identical resonators. Coupling is controlled by means of a pair of patches placed above the resonators. On that same layer, a similar principle is applied towards coupling to input and output ports.

Regarding the lowpass design, the focus is in providing a wide, deep rejection stopband, while the requirements for the sharpness in the transition from passband to stopband are relaxed. The design is intended to be used as a clean-up filter, i.e. cascaded to a previous filter in order to eliminate spurious resonances. The design is based on a pair of coupled lines with an additional feedback, multistepped impedance line.

Chapter 6 presents a summary of the work carried, along with achievements and conclusions.

1.3 Transmission-line concepts

The purpose of this section is introducing some of the concepts on the type of transmission lines that will be used in subsequent chapters, only for reference.

1.3.1 Coaxial transmission line

The coaxial transmission line is the most extended form of transmission line. It is a two-wire transmission line, so it can support TEM waves. The structure is formed by a central conductor (inner conductor), a dielectric surrounding it, and another layer of metal (outer conductor) surrounding the dielectric (Fig. 1.2). The characteristic impedance of this type of transmission line is given by:

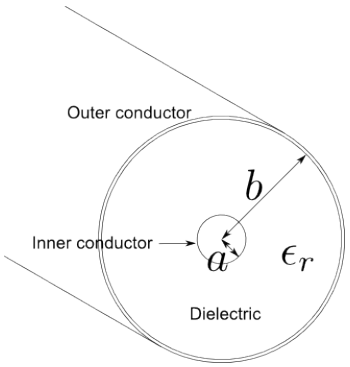

Figure 1.2: Coaxial transmission line parameters

$$Z_0 = \frac{59.96\Omega}{\sqrt{\epsilon_r}} \ln \frac{b}{a} \tag{1.1}$$

where ϵ_r is the substrate dielectric constant, a is the inner conductor diameter, and b is the outer conductor diameter.

1.3.2 Coplanar waveguide

The coplanar waveguide (CPW) consists of a centre metal strip with a width W and two ground planes located parallel to and in the plane of the strip [2], separated by a gap, denoted by G (Fig 1.3). The CPW is printed on a substrate with thickness h and dielectric constant ϵ_r, and the metal layer has a thickness t. This type of transmission line is quasi TEM, as there is a small longitudinal component of the electromagnetic field at the air-dielectric interface [3]. One of the main advantages of CPW is the fact of having both signal and ground on the same plane, making much easier the shunt connection of elements since via-holes are not required in order to reach the ground plane. However, its open nature has the drawback of increased radiation losses, when compared to a traditional microstrip line.

Characteristic impedance of the CPW (Z_c) and effective dielectric constant (ϵ_{re}) depend mainly on the ratio W/G. Equations for calculating these values may be found in [4, 5], assuming the ground planes are much wider than the center strip.

Another practical application is to introduce a conductor backing to the CPW, resulting in a so-called conductor-backed CPW (CB-CPW) or grounded CPW (G-CPW). This conductor reduces the line impedance. However, it can improve both the mechanical strength and the power-handling capability.

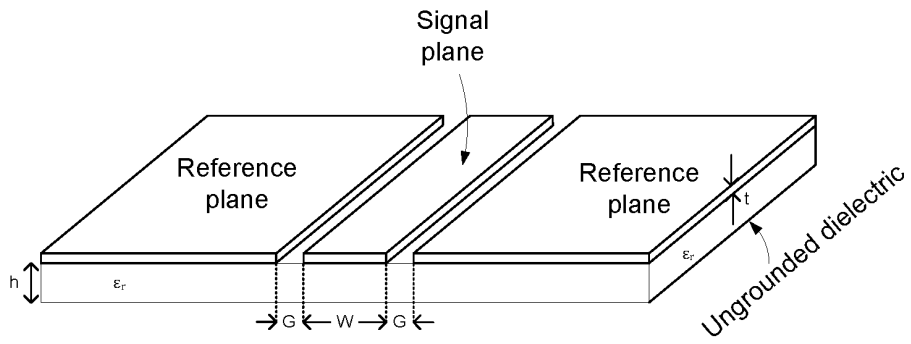

Figure 1.3: Coplanar waveguide (CPW) structure

1.3.3 Coupled lines

Power can be coupled between two unshielded transmission lines when in proximity, due to the interaction of the electromagnetic fields of each line [6]. Coupled striplines operate in TEM mode, whereas coupled microstrip lines operate in quasi-TEM. For the development of this thesis, only coupled striplines are considered, so TEM mode is assumed.

The electrical characteristics of the coupled lines can be determined from the effective capacitances between the lines and the velocity of propagation on the line. Two special types of excitation are considered for the coupled lines: even mode, where currents in the conductors are equal in amplitude and direction, and the odd mode, where the amplitude is the same but directions are opposite. Each of these modes has its own characteristic impedance, Z_e for the even mode, and Z_o for the odd mode. Then, the characteristic impedance for the pair of coupled lines is given by:

$$Z_C = \sqrt{Z_e Z_o} \tag{1.2}$$

Coupling coefficient (k) is a parameter that accounts for how strong the coupling is, calculated as [3]:

$$k = \frac{Z_e - Z_o}{Z_e + Z_o} \tag{1.3}$$

Assuming an equivalent circuit for a pair of coupled lines with electrical length θ (Fig. 1.4), the structure can be defined in terms of its Z-parameters as:

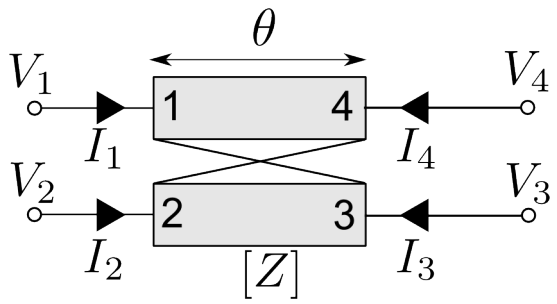

Figure 1.4: Coupled-lines equivalent circuit

$$\begin{pmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{pmatrix} \tag{1.4}$$

$$\begin{aligned} Z_{11} = Z_{22} = Z_{33} = Z_{44} &= \frac{-j}{2}(Z_e + Z_o)\cot\theta \\ Z_{12} = Z_{21} = Z_{34} = Z_{43} &= \frac{-j}{2}(Z_e - Z_o)\csc\theta \\ Z_{13} = Z_{31} = Z_{24} = Z_{42} &= \frac{-j}{2}(Z_e - Z_o)\csc\theta \\ Z_{14} = Z_{41} = Z_{23} = Z_{32} &= \frac{-j}{2}(Z_e + Z_o)\cot\theta \end{aligned} \tag{1.5}$$

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Chapter 2

Multilayer LCP Fabrication

2.1 Introduction

Multilayer circuits provide a significant advantage to conventional circuits by reducing the footprint. However, the complexity of the fabrication process increases as more layers are added. This chapter aims at discussing the fundamentals of multilayer circuit fabrication, and then focuses on the process applied to liquid crystal polymer (LCP). Most of the work carried in the development of the process is part of industrial processes and is not available on the open literature.

This chapter is structured as follows: starting with an introduction to multilayer circuits, then LCP material is introduced, pointing the benefits of using it in microwave circuits. Then, as a starting point to the fabrication stage, the generic process for producing multilayer circuits is described. This process is then adapted to LCP, describing the process as it was used at the beginning of the project, followed by a discussion on what the main challenges are, proposing alternatives in order to overcome them. Based on this, improvements to the process are covered in detail in Section 2.4. The chapter concludes with a summary and discussion of the improvements achieved through the development of this project, as well as suggestions for further improvement that could be applied as future work.

2.1.1 Multilayer technology

Printed circuit boards (PCB) provide mechanical support and interconnection for electronic components. A PCB is formed by one or many metal layers, where the circuit features are patterned, placed onto a non-conductive substrate. According to the number of metal layers contained in the PCB they can be regarded as single-layer, double-layer, or multi-layer (Fig. 2.1).

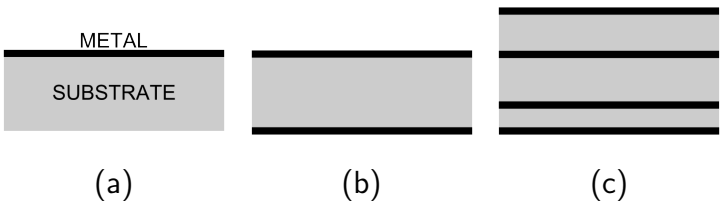


Figure 2.1: PCB classification (a) Single-layer (b) Double-layer (c) Multi-layer

Multilayer PCBs can provide tremendous savings in volume compared to their single- or double-sided counterparts at the cost of increased design and manufacturing challenges. As the space gets tighter, separation between components is reduced, increasing the amount of unwanted coupling between them and, therefore, the design difficulty. Furthermore, the need for including electrical connection between the different layers, increases the challenge in the manufacturing process.

PCBs are commercially available in a copper-clad form, i.e. layers of substrate with one or two sides coated with copper. Fabrication of multilayer PCBs require two components: metal-clad substrate and prepreg material, that acts as a glue to bond layers together. Prepreg can be many different materials and, therefore, have different electrical properties. Depending on the amount of prepreg material in comparison to the substrate, its properties may become dominant in the circuit. It is desirable that the prepreg and the core material have the same properties [1].

In order to form a strong bond between the layers, the prepreg has to go through a curing process, in which the layers are taken through a process of pressure at an elevated temperature. This process is also known as *lamination*. The amount of pressure and temperature required is determined by the prepreg material. During the process, the prepreg would reach a melted state and fill the spaces between the core layers. This is followed by a cooling-down process where the prepreg solidifies, forming a solid block with the rest of the layers.

For circuit patterning, or transferring the circuit design drawing onto the PCB, several methods are available. They can be classified as additive, where the circuit is patterned on the substrate by imprinting the conductive tracks, or subtractive, meaning unwanted parts are removed from a full metal coating leaving the circuit pattern behind.

Additive methods tend to be more expensive and are out of the scope of this project. Regarding subtractive methods, patterning could be done by mechanical milling or chemical etching, the latter being the most commonly used, specially for low-volume or prototyping production. Etching is done in two steps: metal coated with a photo-resist layer is exposed to an UV light, obscuring the parts where metal should remain, with a mask. Then, the board is submerged in a chemical solution that dilutes the parts of photo-resist that have been exposed to light with the metal, leaving the patterned board.

Layers may be connected physically or electromagnetically. The latter does not require a physical connection and does not increase the fabrication complexity, even though it has some drawbacks (see Chapter 3). On the other hand, connecting layers physically is one of the most challenging steps in the manufacturing of a multilayer circuit. This electrical connection is granted through so-called vertical via transitions. Depending on where on the layer stack they are originated and terminated, vias can be classified as through-, when they go from the top layer to the bottom layer, blind-, when one end is open and the other is in one of the inner layers, and buried-, where both ends of the via are located in the inner layers.

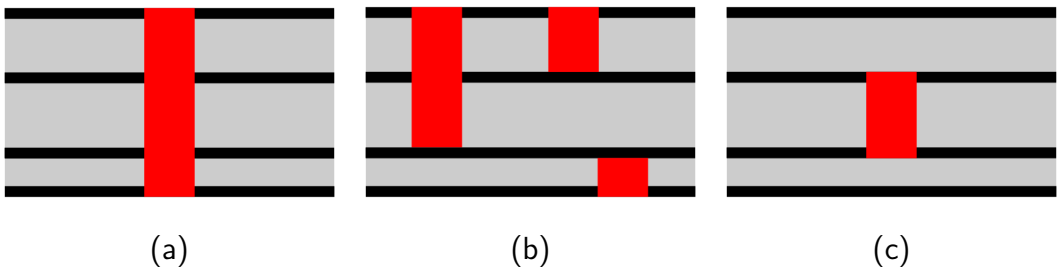


Figure 2.2: Via classification. (a) Through via (PTH) (b) Blind vias (c) Buried via

The via production involves opening, or drilling, the cavity in the substrate and then plating it to make it electrically conductive. Drilling can be done either mechanically or by laser, each of them with its pros and cons. Several alternatives are available for via plating, including the use of conductive pastes and electroplating.

2.1.2 Liquid Crystal Polymer Substrate

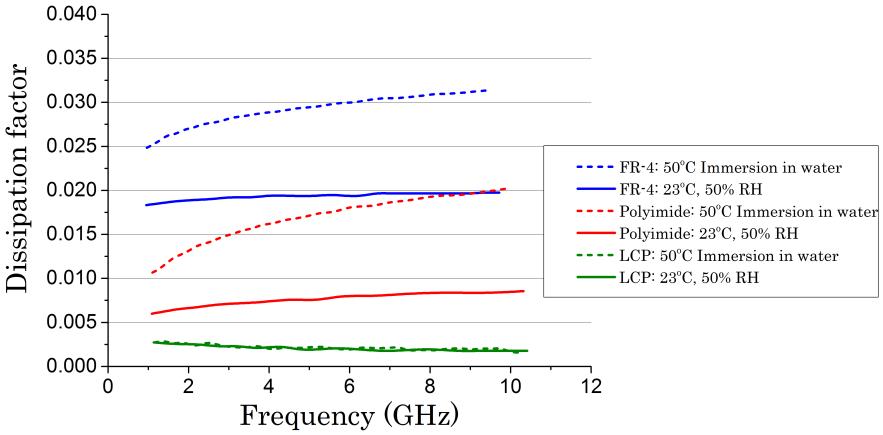
Liquid crystal polymer (LCP) is a thermoplastic material with unique structural and physical properties. Its usage as a microwave substrate was first introduced in the early 1990s [2]. This early form of LCP films presented several challenges that compromised the reliability for circuit production, mainly poor LCP-to-metal adhesion and failure to produce plated through holes (PTH) to electrically interconnect different layers. However, in the last few years, active research has been carried in this field and LCP is now a common alternative to existing microwave materials, not only as a substrate but also as a packaging material.

Since its introduction, several studies have been published demonstrating the properties that make LCP such an interesting material for RF and microwave applications [2–5]. Regarding the electrical properties, it has a low loss tangent ($0.002-0.0045$) and low dielectric constant ($2.9-3.2$). Furthermore, these properties remain stable for frequencies up to up to 105 GHz [2, 5], as opposed to other materials (Fig. 2.3).

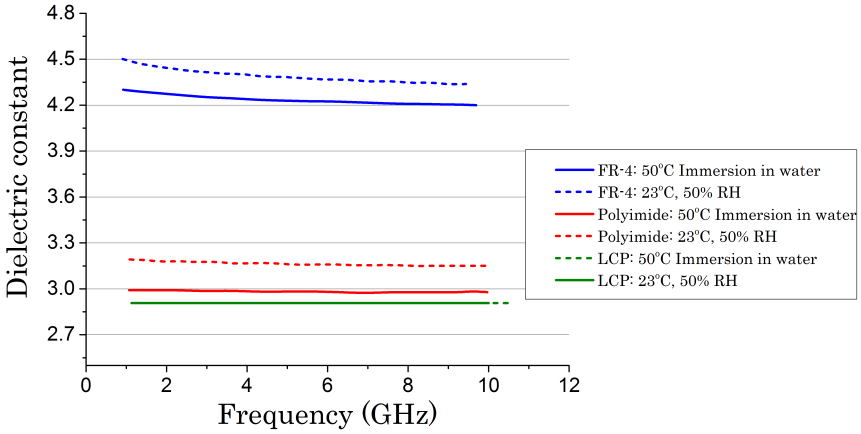
On the mechanical properties side, LCP has low water absorption ($< 0.04\%$) and high chemical resistance, producing a stable behaviour across a wide range of environments. This properties make LCP a good candidate for packaging applications. Also, temperature variations have little impact since LCP has a low x-y coefficient of thermal expansion (CTE). This coefficient is controllable during fabrication (0-40 ppm/°C) so it can match other materials' CTE, like copper (16.8 ppm/°C). Z-axis expansion coefficient is higher, but due to the thin LCP layers, its effect is negligible unless very thick multilayer modules are used [2].

2.1.3 Liquid Crystal Polymer in Multilayer Circuits

LCP substrate is available in two kinds of laminates. Both of them share the exact same electromagnetic (EM) properties [6, 7], with the difference being the melting temperature for each of them. The laminate with lower melting temperature, *bonding film*, can be effectively used as prepreg and bond together higher temperature melting laminates, *core film*. This is an advantage over other materials since all-LCP blocks can be fabricated without introducing foreign materials with different EM properties.



(a)



(b)

Figure 2.3: LCP substrate properties compared to FR-4 and polyimide in the cases of 50 °C water immersion, and 50% relative humidity at 23 °C [6] (a) Dissipation factor (loss tangent) (b) Dielectric constant

The most common technologies used for multilayer circuits are thin-film PCB, LTCC [8], and LCP. Thin-film PCB and LTCC are well established, mature technologies, whereas LCP is still in development. However, LCP has the advantages of lower price and less demanding fabrication facilities, as well as being lighter in weight. Furthermore, LCP is also employed as packaging material [9, 10].

2.2 Initial fabrication process

In this section, the process and equipment used are covered, as a starting point for the project. The process is based on previous in-house experience and substrate provider recommendations, comprising chemical etching for circuit patterning, laser-drilling for via production, and a thermal-compression lamination process.

2.2.1 Circuit patterning

Copper-clad layers of LCP are available in different thickness: 25 and 50 μm for bonding film, and the same for core film, plus 100 μm. These layers are also availabe with UV-sensitive photo-resist coating. The method used for circuit patterning is standard PCB chemical etching method with photoengraving. A photo-mask is applied on the board with the circuit pattern and then exposed to UV light for a certain time. The board is then submerged in an etching solution that removes the parts of the copper that have been exposed to light. The circuit is patterned on core film layers, while bonding films are used only as adhesive layers.

Masks are produced using an ink-jet printer and transparent film. Apart from the circuit itself, the mask also contains some other elements that are needed for multilayer fabrication, mainly for vertical alignment of the layers. The mask design comprises three pins for vertical alignment. In some cases, a double-sided mask may be required, i.e. a mask that would be applied to both sides of an LCP layer at the same time, requiring accurate alignment. This is achieved with the help of thin lines printed surrounding the mask content (Fig. 2.4) and manually aligned under the microscope and bonded together, leaving an opening for the access of the LCP layer.

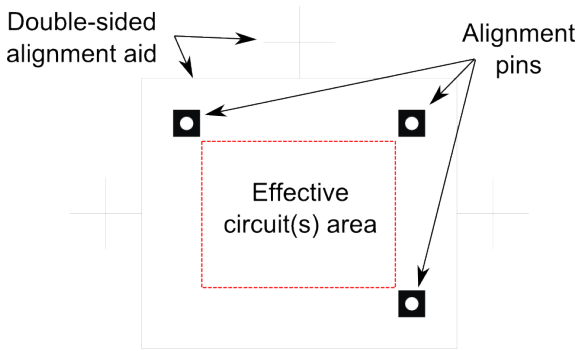


Figure 2.4: Initial mask

2.2.2 Layer conditioning

Next step after the circuit patterning is preparing the different layers for vertical alignment and lamination. Etched alignment pins are laser-drilled on core films, and then used as a template for drilling the same holes on bonding film. After drilling, surface of every layer is rubbed with isopropyl alcohol (IPA) to remove any rests of lasing. Lastly, before proceeding to the lamination, the boards are cured for one hour in the oven at 150 °C to eliminate any trace of moisture.

2.2.3 Lamination

Lamination is the process through which the different layers containing the etched circuit and the adhesive layers are bonded together to form a solid LCP block. This process is the equivalent to prepreg curing described in previous sections. The LCP layer stack is taken through a thermal-compression process that nearly melts the bonding film and glues the core layers together.

For the lamination process, two plates are used as a holder for the layer stack. These plates are made in-house with 1 cm-thick steel. They have 3 alignment points with an effective area, i.e. area within the alignment pins, of 5x4 cm^2 (Fig. 2.5). Steel is flat, solid, and good temperature conductor so quickly can transfer the heat from the external plates to the LCP with little delay, allowing a better control over the time the material is exposed to a given temperature. To prevent LCP to stick to the steel, the plates are pre-treated with a coat of lubricant. A pair of spacers with the same thickness as the LCP stack are placed on the sides in order to prevent over-compression of LCP.

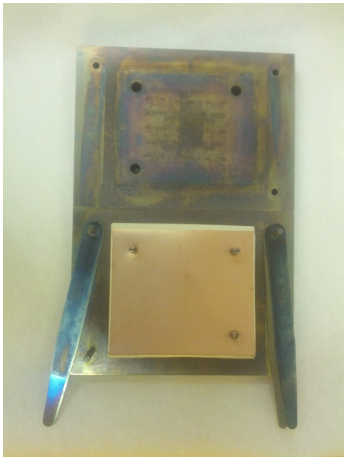


Figure 2.5: Steel plates

With the layer stack ready, the plates are placed in a heated press for lamination. The thermal-compression cycle used is plotted in Figure 2.6. As LCP is heated up, it expands. Expansion in the vertical axis (Z-axis), increases the pressure between the plates. This requires an adjustment on the pressure applied every 4-5 minutes in order to keep the lamination pressure constant, with special attention during the high-pressure stage.

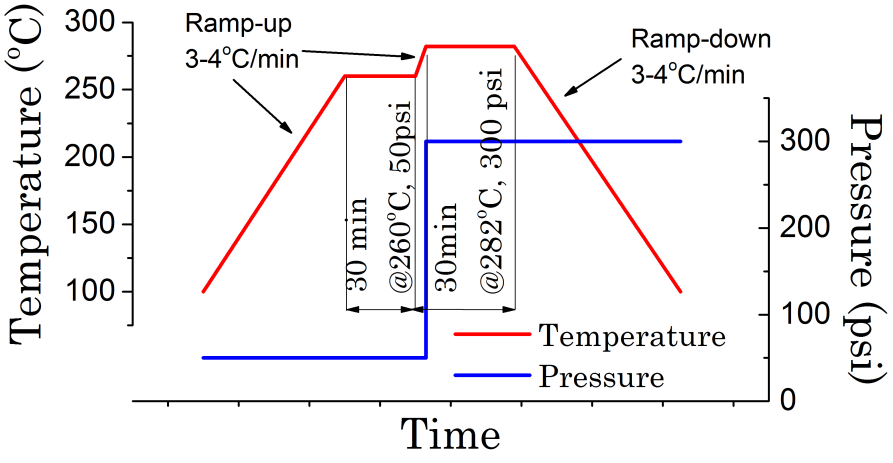


Figure 2.6: Substrate-provider recommended lamination cycle [11]

2.2.4 Layer interconnection

Via holes are drilled with a CO_2 laser. Laser melts and burns LCP as it goes through, leaving residue behind that needs to be cleaned before plating the via hole. The cleaning process is carried by submerging the laminated block in IPA and then

rubbing the surface with a soft material.

As previously mentioned, one of the aims of this project is to keep fabrication costs to a minimum. For this reason, standard PCB plating techniques with commercially available LPKF ProConduct kit [12] are used. The method consists on applying a layer of conductive paste on one side of the board and apply vacuum on the other. The paste will then flow through the via hole adhering to the walls and establishing an electrical contact between the ends. The process is repeated on the other side of the board. This technique can not be applied to plating blind via holes as there is not an open way for the air to flow through. However, for shallow vias, applying paste on the surface and then squeegeeing it with an applicator, provides good results for the via depths covered in this project (< 600 μm). Finally, conductive paste needs to be cured for it to settle and solidify.

2.2.5 Fabrication steps

A summary of the previously described fabrication steps is sketched in Figure 2.7.

2.3 Fabrication process analysis

Initial experiments following the previously described fabrication method suggested some flaws that needed to be addressed. First, a tolerance analysis is required in order to determine the limits of the process and bring that information into the design stage, so the fabrication errors can be compensated for or, at least, delimited. Secondly, lamination process and layer interconnection proved to be unreliable and inconsistent through experiments, in terms of bonding strength. Applying excessive pressure leads to inter-layer misalignments and over-compression, while applying little pressure produces fragile devices.

2.3.1 Circuit patterning tolerance analysis

When studying the tolerance of the circuit patterning process, mask and etching must be considered in combination. As previously mentioned, masks are produced with an ink-jet printer on transparent film. A close look at the printing accuracy

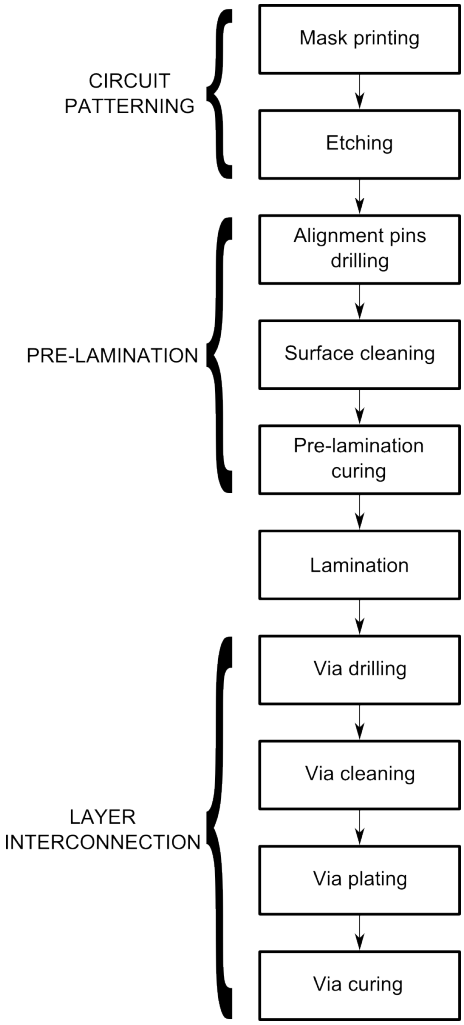


Figure 2.7: Initial fabrication process

suggests a better definition of circuit features when printing horizontally, in relation to the printing direction. On the other hand, when printing vertical features, edges lack sharpness (Fig. 2.8). This represents a limitation in the quality of a transmission line, since its characteristic impedance is affected by variations in its width, meaning it will not be stable across its length. The effect has a greater impact on the result as thinner lines are printed, placing a fabrication limit.

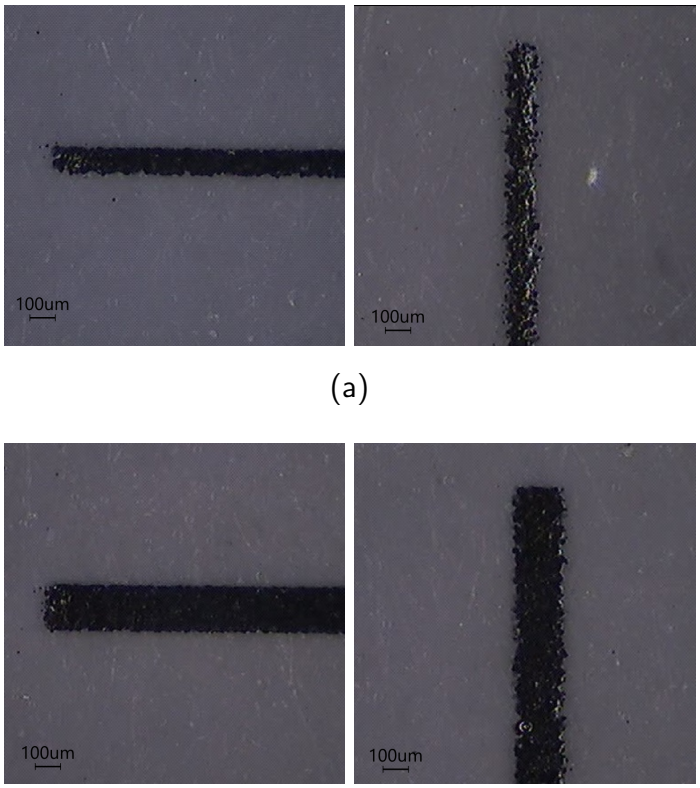


Figure 2.8: Mask printing accuracy on horizontal and vertical axes (a) 100 μm wide line (b) 200 μm wide line

Ink-jet printers often offer more resolution in dots per inch (dpi) than laser ones, however, because ink-jets work by squirting very small quantities of ink onto paper, the ink ends up spreading in the paper as it dries. This can sometimes give their printouts a less crisp appearance than laser printers. Furthermore, while laser printers will generate about the same quality of output with any standard office paper, ink-jets are more sensitive to paper quality as well as to the humidity level in the air.

With the available kit, measured prints show features being wider that expected by a few microns, as well as circles for via holes are smaller on diameter. However, etching compensates for this dimension increase, and through the experiments carried along

the project, the combined tolerance mean value is ±30 μm. As an example, when designing a 300 μm-wide line, its width after etching would be in the range of 270-330 μm.

Further experiments were also carried in order to establish the limit for the thinnest line, being 150 μm. Etching lines thinner than that limit would produce lines with very inconsistent characteristic impedance, as well as electric cuts along the path. In order to increase the yield of the fabrication process, the minimum width of a line at design stage is fixed to 200 μm.

Given the previous discussion, at design stage, the 30 μm tolerance must be considered and, in order to produce a line with accurate dimensions, it is convenient to produce a mask with wider lines. An example is shown in Figure 2.9.

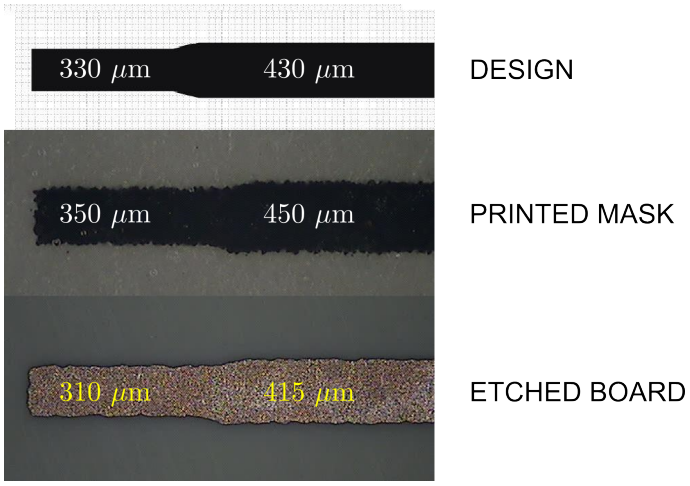


Figure 2.9: Circuit patterning tolerance

2.3.2 Lamination discussion

Lamination is a critical step in the fabrication process. Circuit thickness, alignment, and bonding strength all rely on it. Therefore, the lamination cycle has to be carefully designed, choosing the right values of temperature and pressure that would provide a bonding sufficiently strong, while not deforming the core layers. The key property to look at for this matter is LCP's storage modulus, defined as the ratio between the stress force applied to an elastic material per unit area, and strain, the proportionate change produced in some length parameter. The lower the storage modulus, the softer the material is and, therefore, easier to deform under

a certain load. Furthermore, successful lamination cycle settings would be those making bonding film soft enough to reflow and fill the gaps with the core film, while keeping core film strong enough not to lose its original shape. As LCP's storage modulus is a function of temperature and is different for bonding and core films (Fig. 2.10), values for temperature and pressure have to be carefully chosen.

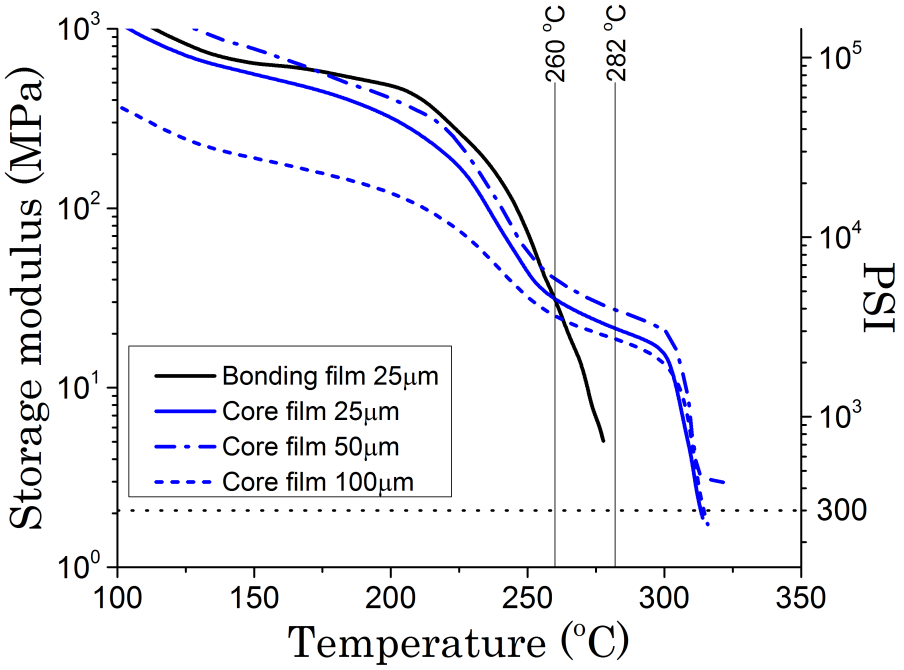


Figure 2.10: LCP storage modulus for different types of laminates [11]

When using the initial lamination cycle (Fig. 2.6), the critical high pressure stage uses 282 °C. At this point, bonding film's storage modulus is below core films'. However, the problem resides in the proximity of the core films to their melting point ($\sim$ 300°C), where the storage modulus plummets dramatically. Considering bonding film's storage modulus needs to be lower than core films', that reduces the temperature window to a range from 260 to 300 °C. Effectively this window is narrower as melting point needs to be safely avoided and core films' storage module must be substantially higher than bonding film's. Therefore, accurate temperature control is critical in the lamination process and oil heated plates are recommended for that purpose rather than electric ones, which tend to overshoot.

Different lamination settings have been tested, including lower temperatures with increased pressure, as reported in [13]. However, quality problems were recursively found, due to either over-compression or over-heating, in the form of inter-layer misalignment, broken lines, and unwanted variations in the shape of circuits (Fig.

2.11). All these problems are related to the proximity of core film to its melting point.

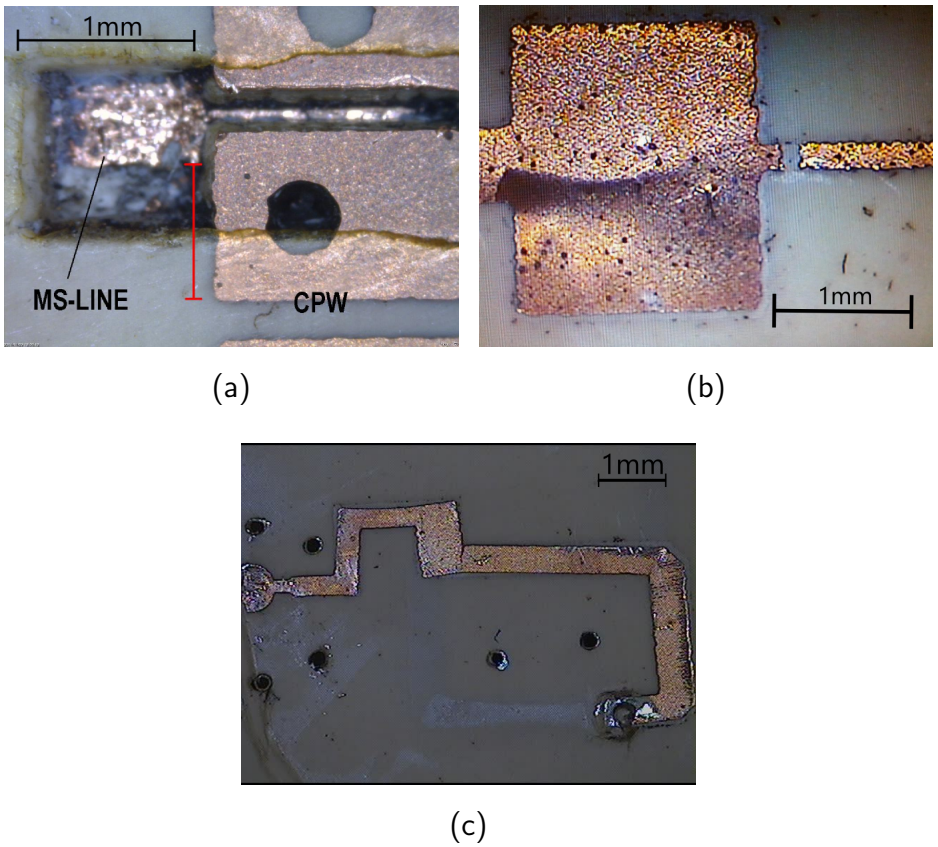


Figure 2.11: Lamination errors (a) Inter-layer misalignment (b) Snapped line due to over-compression (c) Circuit shape distortion

Furthermore, when considering the vertical axis, it has been also found how the patterned circuit gets embedded in the substrate. The copper thickness is around 10 μm and, should this be negligible when dealing with thicker substrates, it is quite significant when applied to 25 μ. If the copper gets embedded into the substrate, the thickness, or the distanced between the metal layers, would be reduced by 10-20 μm, which can be quite a significant error when working with very thin layers of 25 μm.

Also critical in fabrication is the thickness tolerance. Substrate provider states a tolerance 10% for its bonding film [7]. This value is relative, as the overall thickness of the circuit will highly rely on the lamination process. As such, pressure control during the lamination process is critical, specially during the high-pressure stage. Available equipment relies on a manual adjustment of the pressure and needs to be continually supervised.

Reported problems can be found either across the entire laminated area or sometimes in localized areas of the circuit, as areas where more layers of copper are aligned vertically receive more pressure than the rest. Therefore, it is of high importance to distribute the pressure evenly across the whole surface.

2.3.3 Layer interconnection

After running several experiments it is found that one of the main difficulties is accurately positioning the laser beam over the area that needs to be drilled. Since the laser does not have a fiducial camera, this has to be done manually and is error prone. Lack of self-alignment capabilities of the laser prevents bulk drilling of the vias so they have to be done on a one-by-one basis, which is time consuming.

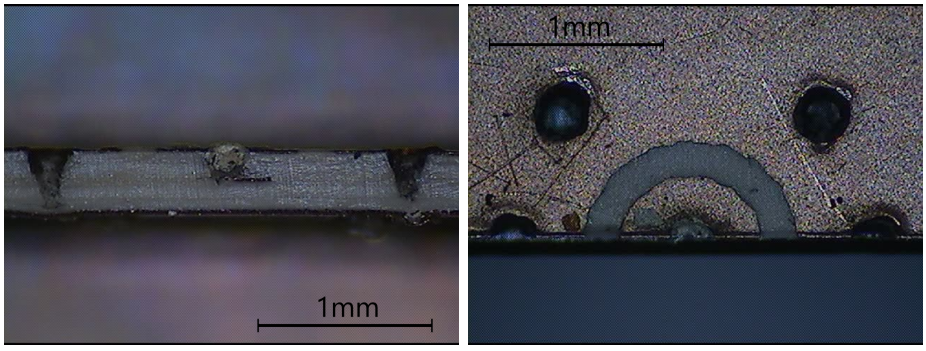


Figure 2.12: Laser drilled vias with conical shape. Circuit cross section on the left, and top-view on the right.

Laser drilling produces vias with a conical shape (Fig. 2.12, left). Depth of the drilling depends on the diameter of the via opening. As the via size investigated during this project is as narrow as 200 μm, the depth limit for laser drilling is in the range of 500 μm. For through vias beyond this limit, drilling from both sides of the board is required.

As discussed, after drilling, cleaning of the via cavity is required prior to plating. This proved to be the most challenging step at this stage. Blind via holes with an opening diameter $>$ 500 μm allow for easy access to the bottom of the via. However, when the diameter is reduced to 200$-$300 μm, a surface cleaning is not enough. Alternatively, an ultrasound bath was tested showing little improvement.

Additionally, as the fabrication process stands, there is no procedure nor tests done

for producing buried via holes. This limitation needs to be addressed as it is necessary for fabricating fully packaged filters.

2.4 Fabrication process development

Given the challenges discussed in the previous section, the aim of the project in this area is set to obtaining a fabrication process that is able to produce reliable interconnections, using vias as narrow as 200 μm, as well as producing buried via holes.

As previously stated, one of the main difficulties in producing reliable connections is the cleaning of blind via conducts with narrow diameter. Furthermore, having a residue-free end of the via is essential so the conductive paste is uniformly distributed, providing a good electrical connection. Given the cleaning methods such as surface cleaning or ultrasounds bath do not fulfil the requirements, an alternative method is proposed. The idea is, instead of cleaning the vias after drilling them, to produce them clean and eliminate the need for the cleaning step. To achieve this, every circuit layer is processed and drilled independently and then put together for lamination. The result is a via conduct ready for plating straight after lamination, avoiding any intermediate steps. In this case, vias have a cyclindrical shape, rather than the conical shape obtained with the laser drilling.

Advantages of this method include a reduction in the number of stages required for fabrication, as well as combining the alignment holes drilling with the via drilling, making the use of the laser more efficient, and then surface clean of the layer would be sufficient to have it ready for lamination. Another advantage is making the process modular in the sense of every layer can be quality checked independently and replaced, if needed, before the lamination. In order to successfully develop this fabrication process a combined improvement of lasing, mask, and lamination needs to be put in place.

2.4.1 Laser processing

Processing individual layers of LCP with laser is a delicate step due to its thermoplastic nature. Low power needs to be applied so LCP does not melt in excess. This low power is combined with high-frequency pulses and several repetitions to cut through the layer.

As important as the power settings is the setup of the layer for drilling. First experiments were carried by holding LCP layers with adhesive tape on the edges. It was found that even with low-power laser, LCP melts and re-flows following the laser direction (Fig. 2.13), compromising the layer-by-layer process, as the roughness of the end of the via would affect its positioning in relation to adjacent layers.

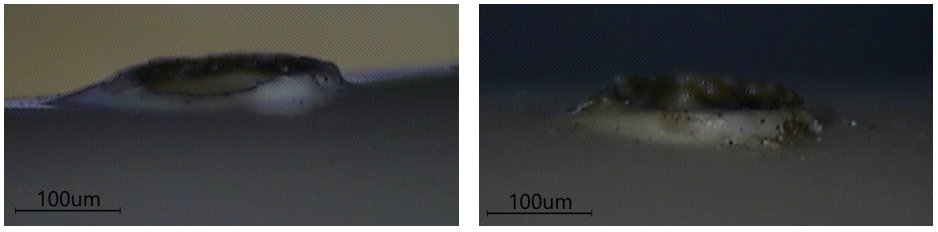


Figure 2.13: Detail of 200 μm diameter laser drilling. (a) 50μm bonding film (b) 100μm core film

Solution to this was mounting the LCP layer on a copper, flat board and use adhesive over the whole LCP surface to achieve a tight contact between them. Several adhesive coating solutions were tested for this purpose, even though the residue left on LCP layers lead to discarding this method. Instead, a thin layer of water was used. Water has adhesive properties, it is not flammable, and does not leave any residue. Spreading a small amount of water on the copper and compressing the LCP layer against it to remove any air bubbles, provided results with significant reduction of the LCP reflow (Fig 2.14).

Via cavities are product of the vertical alignment of concentric circles cut on every layer. As such, the lasing process involves the cut of circles of different diameters on each layer, including alignment holes. Even if low-power is applied, a certain degree of melting is expected, making the laser pattern to have a certain width on the LCP. This results in drilled circles being wider than the original design by 100 μm, approximately (Fig. 2.15). Width excess must be compensated by adjusting

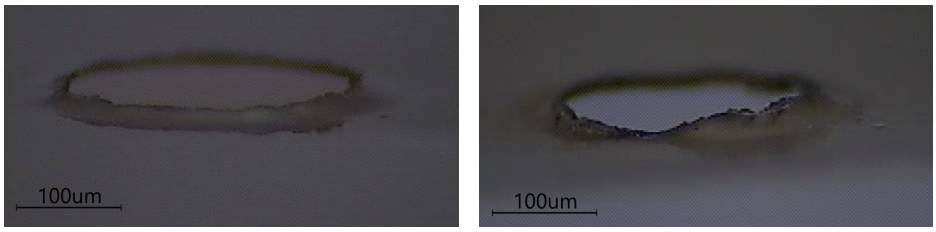


Figure 2.14: Detail of 200 μm laser drilling with adhesive layer of water. (a) 50 μm bonding film (b) 100 μm core film

the drilling dimensions.

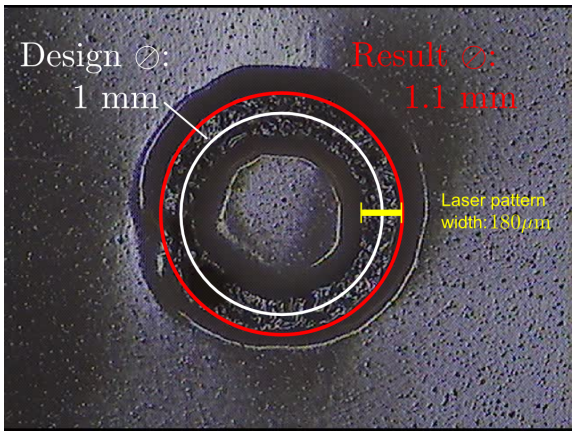


Figure 2.15: Effects of laser drilling on LCP

2.4.2 Mask

One of the main problems during fabrication was the pressure distribution across the circuit surface. Even though this is largely affected by the lamination process, the design of the mask also plays a key role for this matter. As such, different patterns for the non-circuit areas of LCP layers are investigated and incorporated to the initial mask design (Fig. 2.4). At first, a solid frame of copper surrounding the circuit area was tried (Fig. 2.16), with results showing a more uniform pressure distribution. However, pressure applied on the copper frame pushes LCP towards the circuit area, producing misalignments due to the lateral forces.

Alternatively, a patterned frame was investigated as a double layer, where the solid frame of copper from the last experiment is replaced by circular patches distributed over the two sides of the layer in a way they do not overlap (Fig. 2.17). Results show

significant improvement compared to the previous iteration. As well as improving the pressure distribution, this mask design also includes a set of benchmark lines to assess the etching quality, assuming the same etching quality across the entire layer. In this way, after etching, benchmark lines can be measured and the layer can be validated or discarded depending on the etching accuracy.

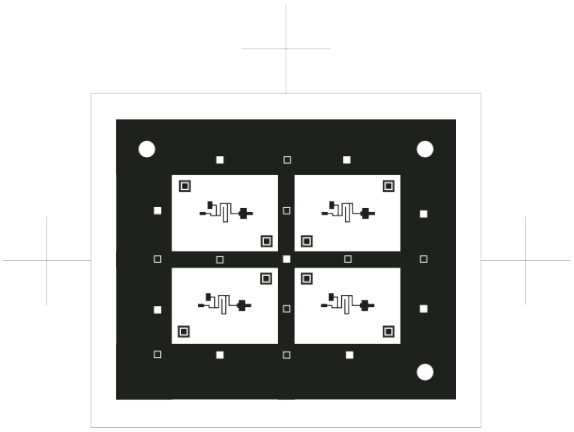


Figure 2.16: Mask variation. Copper frame surrounding circuit area for improved pressure distribution

2.4.3 Lamination

First step for improving the lamination process was to eliminate the use of spacers, as they were preventing a real control of the pressure applied on the LCP layers and the development of an appropriate lamination cycle.

Even though lubricant coating was efficiently keeping LCP from sticking to the steel plates, it proved to be a problem when performing subsequent laminations, as it would reduce the bonding strength between the layers that had been in contact with it during the first lamination. Therefore, lubricant was replaced by conventional aluminium foil, adding three layers at top and bottom of the layer stack. These extra layers, apart from isolating LCP from the steel plates, also work as a cushion, contributing to a better distribution of the pressure.

With this two modifications in place, different combinations of pressure, temperature, and time were attempted. Finally, the lamination cycle producing optimal bonding results was found by modifying the original one to a much lower pressure, 100 psi (Fig. 2.18).

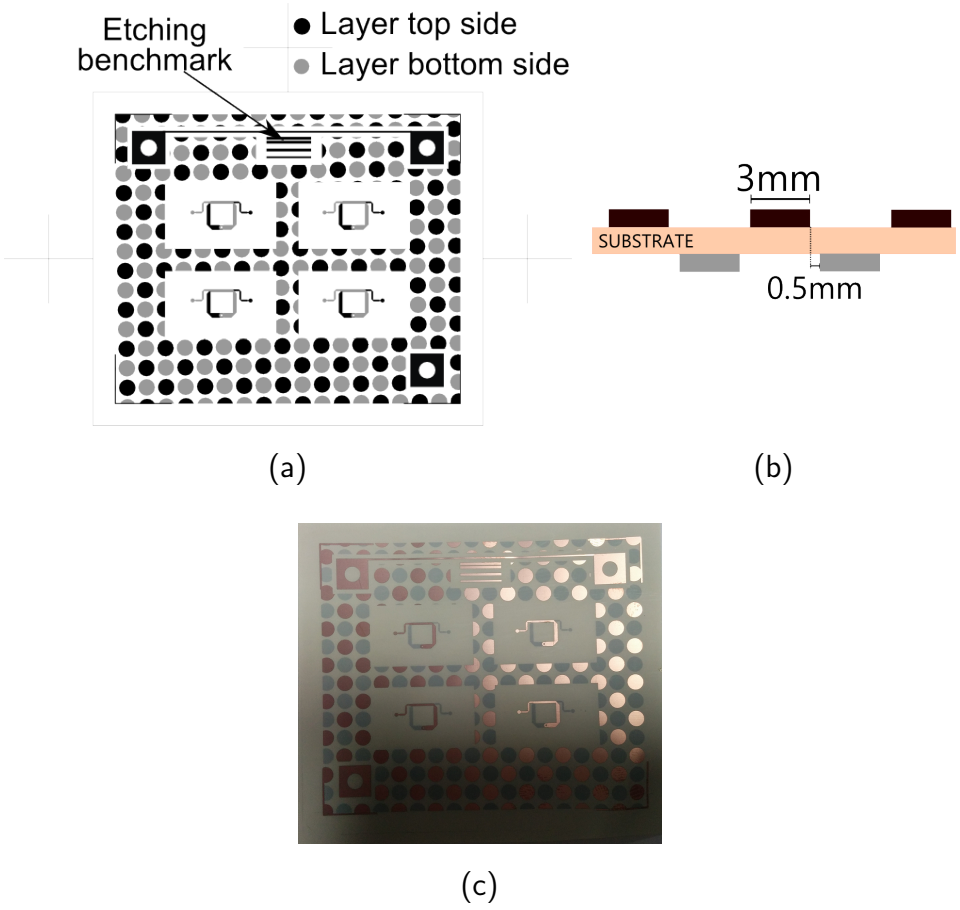


Figure 2.17: Final mask variation. Copper patches distributed around the circuit area on both sides of the layer. (a) Mask design (b) Side-view (c) Etched on 25μm substrate

2.4.4 Buried via production

Solution for producing buried vias is to include an additional lamination process. Firstly, the group of layers through which the buried via would span, are laminated and plated as if it was a final product with through vias. Then, on a second lamination process, the rest of the layers to form the final circuit are included and taken through a new lamination process (Fig. 2.19). This process has been tested providing good results, regardless the number of layers forming the pre-laminated part.

2.4.5 Optimized fabrication process steps

A list of the fabrication steps comprising the optimized process is sketched in Figure 2.20.

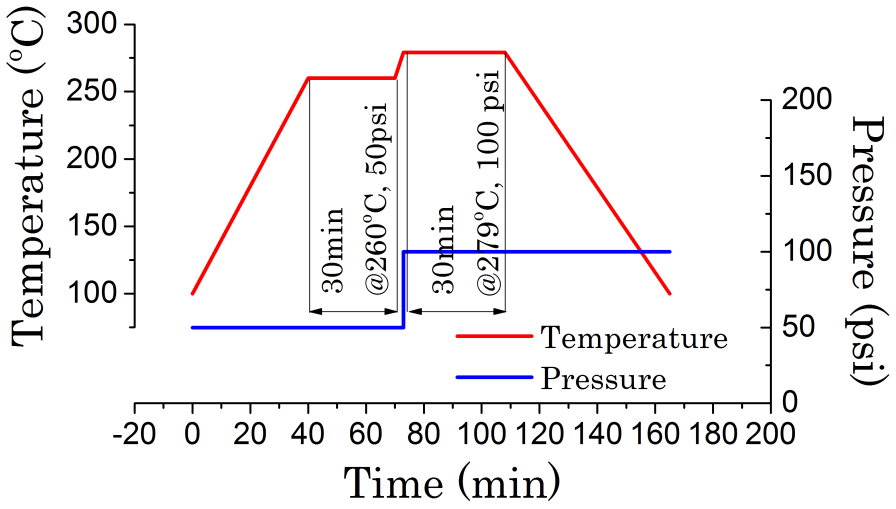


Figure 2.18: Optimized lamination cycle

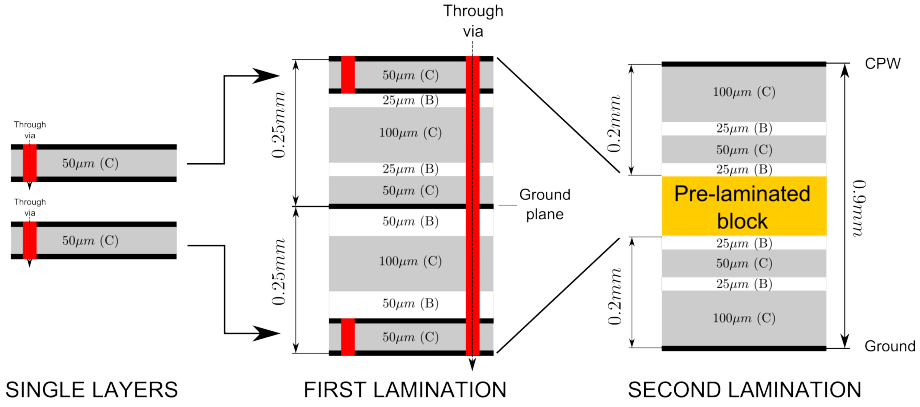


Figure 2.19: Buried via fabrication process example

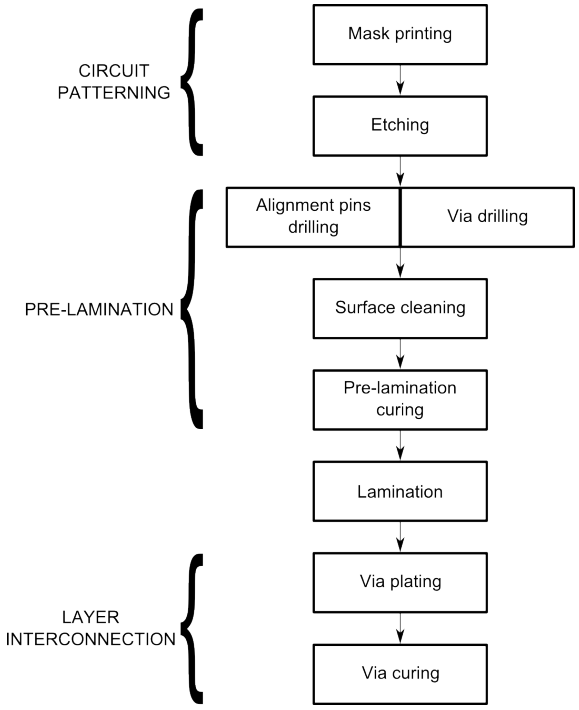


Figure 2.20: Optimized fabrication process

2.5 Conclusions and future work

In this chapter the fabrication process has been covered. Initial fabrication process has been described and analysed, pointing its limitations and flaws. Based on this analysis, improvements have been put in place, as well as finding a tolerance value for the circuit patterning of ± 30 μm on the x-y plane. It has also been demonstrated how to produce and plate through, blind and buried via holes.

Nonetheless, the main improvement to the fabrication process is moving from a post-lamination via drilling to a pre-lamination one. The advantage being eliminating the difficulties of cleaning the inside of blind via holes after lasing, and combining in the lasing stage both alignment and via production. Furthermore, as every layer is treated individually, the process is more modular and allows for better quality control, as faulty layers can be replaced without discarding the whole stack.

The use of the laser has also been optimised, moving from a system where the laser had to be aligned for every single cavity, to a method where the whole layer is aligned only once and all the lasing is done automatically.

Even though the new process is providing good results, experiments show how the pressure distribution across the circuit surface is still not completely uniform. Figure 2.21 shows a picture of a set of filters fabricated following the optimized process. It can be appreciated how through holes are open on the two samples at the top, with the bottom-right one having them closed. This is probably due to the absence of a fourth alignment pin on the corner of the steel plates that would contain the LCP as its storage modulus decays, and the material tends to flow towards that direction.

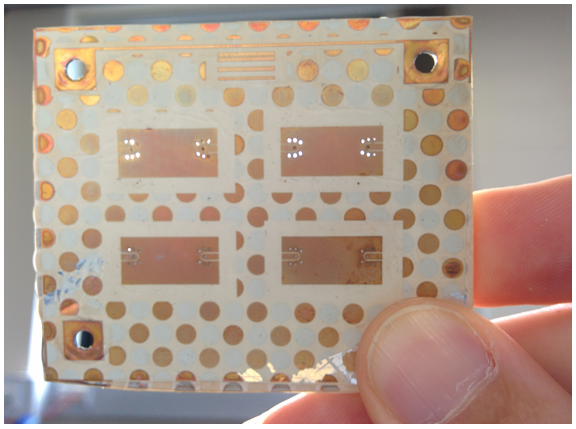


Figure 2.21: Example of circuit fabricated with optimized process

In order to overcome this problem, the author suggests a modification to the steel plate design, including two extra alignment pins distributed asymmetrically next to the open corner (Fig. 2.22). These two extra alignment pins would act as a holder, preventing excessive flowing of LCP.

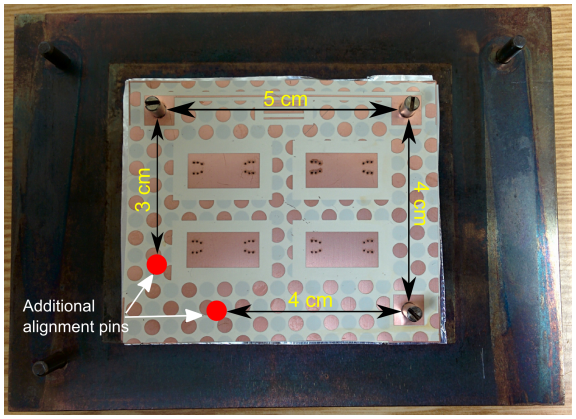


Figure 2.22: Suggested modification to steel plates

Regarding the materials used, during the development of this project, new types of core film laminates were commercially released. Main difference with the ones used is the melting temperature and storage modulus (Fig. 2.23). The potential advantage of using these new materials is widening the temperature window required for lamination, as the storage modulus difference between bonding film and core film is increased at least by one order of magnitude. Therefore, according to the specifications, using these laminates should improve and make more stable the results of the lamination process.

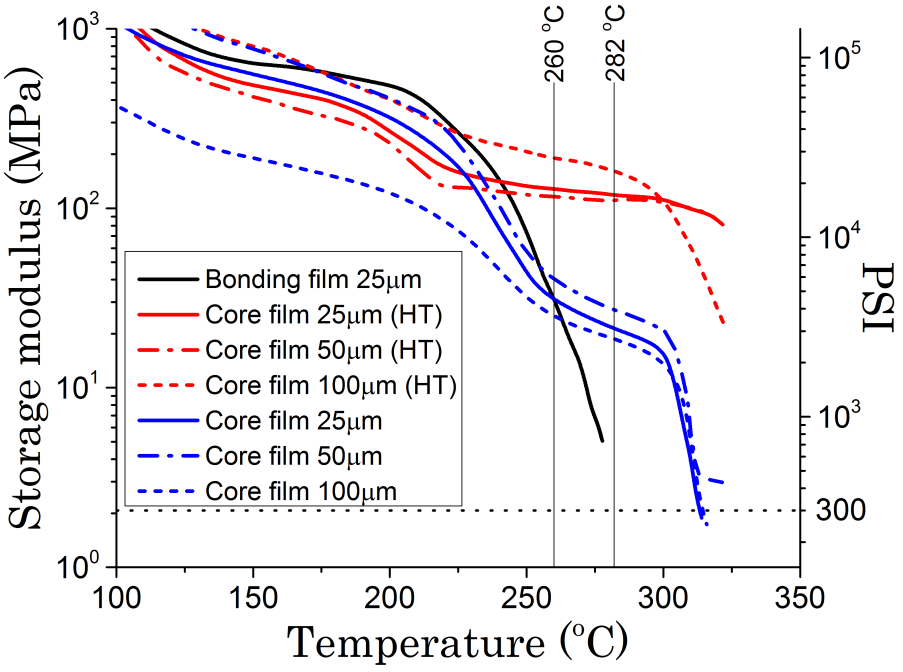


Figure 2.23: LCP storage modulus compared to new high temperature (HT) laminates [11]

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Chapter 3

Vertical transition and packaging

3.1 Introduction

RF and millimetre systems will often have to work in hostile conditions of temperature and humidity, hence the need for a package that protects the system from the environment. Packaging has been a very active research field for many years, and the introduction of materials such as LCP have opened new paths for investigation in this area. LCP has mechanical properties such as low water absorption and high resistance to chemicals and temperature changes that make this material a good candidate for packaging solutions. Even though, manufacturing of this kind of solutions is still at an early stage.

Traditionally, packaging of filters has been a task separated from design, as work reported in recent years tend to use generic, pre-fabricated packages. This type of solution, even though it provides isolation and has little impact on the overall performance of the system, increases the size and weight of the final system, as well as the cost.

The aim of this chapter is to develop a packaging solution that is integrated as part of the design stage and also integrated in the filter fabrication process. This package has to provide similar performance to that of pre-fabricated packages in terms of environmental and electromagnetic isolation. Furthermore, interconnection to the rest of the components in the system has to be simple and reliable.

Successful development of this type of package would provide bespoken solutions

for every filter design, allowing for optimized use of the volume and footprint, and weight reduction.

3.1.1 Background

Two different approaches are found in the literature for integrating and packaging wireless radio components: system-on-chip (SoC) and system-on-package (SoP). SoC has low RF performance and low substrate isolation due to semi-conducting properties. Alternatively, SoP integrates the RF/analog circuitry in silicon and use low loss dielectric to implement components such as filters, antennas, baluns, etc. [1]. Due to the ability of LCP for being used as both packaging material and substrate, most of the recent publications in package integration using LCP follow the SoP approach.

In [2], fabrication methods and measurements are shown for a LCP package with an air cavity. The effects of placing an extra layer of LCP on top of the substrate to form the package are discussed for a conductor-backed coplanar-waveguide (CB-CPW) transmission line. It is shown that placing this extra layer has little or no impact on the results, regardless this layer containing an air cavity or not. In a different experiment, a MEMS is built using an air cavity. Then, pressure is applied to simulate a lamination process revealing little variation with the original results. This opens the possibility of integrating more layers in the same device.

A different line of investigation for LCP packaging is Quad-Flat No-Lead (QFN) packages [3–5]. QFN is a surface mount technology that provides interconnection to the outer world for the contained sub-system, as well as providing isolation. The replacement of typical plastic materials with LCP is leading to QFN packages with low insertion loss and high frequency response.

Work carried in [3–5] show design and measurement results for different QFN packages. Experiments are carried by placing amplifiers [3, 5] and transceiver module [4] and comparing the packaged against unpackaged results. All the packages show an insertion loss better than 0.5 dB, [4] for an 8-20 GHz frequency span, whereas [3, 5] cover from DC to 40 GHz. In [3] hermeticity tests are also carried, showing a leak rate of 3.6×10^{-8} atm cc/s.

Even though this kind of packaging show good results in insertion loss and isolation over a wide range of frequencies, the use of pre-fabricated packages increases the cost of the final solution and places dimensional restrictions to the contained system.

3.2 Vertical signal transition

One of the critical aspects of a packaging solution is the design of its interface, i.e. how the outer environment or host system is connected to the contained device. Assuming a multilayer device, this translates on how to connect the inner layers to one of the external layers, that will act as the interface layer. Signal transition between layers, or vertical transition, can be done using two different techniques: using plated via-holes to physically connect two points (electrical contact), or using electromagnetic coupling, where physical connection is not required. Via-holes have the advantage of being compact and broadband, but the vias introduce parasitic inductances and are difficult to fabricate. On the other hand, via-less transitions are easier to manufacture, but are narrow band and larger in size [6].

As multilayer technologies are more and more used, the need for interconnects with low insertion loss and high bandwidth is also increasing. Several reports cover the topic showing different topologies and approaches.

In [7] a CPW-to-CPW transition is presented using a three-layer stack. The signal transition between layers is made through via-holes (100 μm deep, 200 μm and 150 μm diameters). Results for back-to-back transitions are presented, as well as for open-ended and short-circuit-ended, in the range of 50 to 75 GHz. [8] shows several experiments on single-layer, double-side LCP using different configurations and thicknesses. Vertical transitions CPW-to-microstrip and GCPW-GCPW are tested, showing the latter better results in frequencies up to 40 GHz. The diameter of the vias used also affect the response, being more convenient the use of wider vias. Fabrication process involves some copper and titanium sputtering. Also the dimensions of the lines is quite challenging for fabrication due to its narrowness.

In [9] a back-to-back transition experiment is reported. The experiment consists of a CPW-CPW-microstrip transition using a tapered ground for the intermediate CPW and shows good response up to 100 GHz. Even though it is stated as easy-to-

fabricate, the dimensions of via diameters (150 μm) and line spacing (85 μm) would lead to difficulties in the etching and hole plating process.

In the search for better performance and wider bandwidth, some other work has been carried using several layers for the vertical transition [10, 11]. The work in [10] introduces two different configurations, each of them using four layers for the transition. Good results up to 100 GHz are achieved. However, the use of four layers to implement a vertical transition makes this design impractical for manufacturing. Likewise, in [11] a multilayer transition is analysed from DC to 20 GHz. However, it requires five metal layers per transition, as well as a large number of vias, making this design not convenient for manufacturing.

A vertical transition without vias would bring much ease to the fabrication process. However, the dimensions required to achieve the coupling between layers are higher and the bandwidth of this type of transitions is smaller than those obtained with a via-hole. The work in [12] uses a cavity etched in conductor material to obtain the coupling between top and bottom miscrostrip lines, also using two ground layers between each microstrip line and the cavity. In [6, 13], simplified versions of the previous approach are presented, using only a ground layer between the microstrip layers. This latter version offers not only good improvement for the fabrication process, but also a wider bandwidth while maintaining the insertion loss.

3.3 Package design

Initial requirements for the packaging are:

- Works up to 20 GHz
- Low profile, comparable to a conventional PCB
- Integrated with the filter design, so volume is used efficiently
- Capable of integration with current fabrication technologies
- Able to work in adverse, harsh environmental conditions.
- Provide full electromagnetic isolation
- Light weight

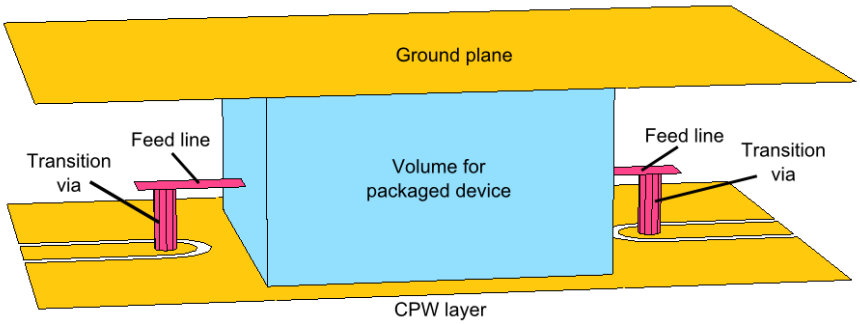


Figure 3.1: Package concept

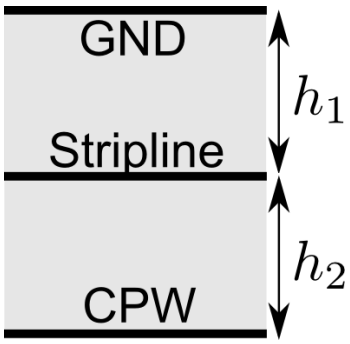


Figure 3.2: Package layers

- Cost efficient

Given the requirements for small footprint and wide band, the use of vialess transitions is discarded. Furthermore, a vialess transition does not provide DC connection so, strictly speaking, it would not be suitable for low pass applications. Based on this, the preferred approach for a transition between CPW and stripline, is a direct via connection.

The investigated solution is intended for circuits with low profile, comparable to that of a PCB. Therefore, main sources of radiation are top and bottom sides of the package, rather than the side walls. As the package needs to be EM shielded, these two sides need to be covered with metal. Both are used as ground planes, so the hosted circuit needs to be designed in a stripline configuration. Even though the surrounding walls are expected to produce little radiation due to the low profile of the circuit, this radiation needs to be minimized. Two approaches are considered: a row of ground vias placed along the circuit edges, and covering the walls with conductive paste in a similar fashion as designing a substrate integrated waveguide [14]. The former was chosen due to the fabrication simplicity.

Another key requirement for the packaging is providing ease of interconnection, something similar to QFN, that allows flip-chip connection to a host board. CPW is a type of transmission line that has both signal and ground on the same plane, making it a good candidate to act as an the interface between the packaged device and the host board. When placing two sections of CPW on one of the ground planes of the packaging, some radiation is expected, mainly from the signal part of the CPW. However, the gap between signal and ground can be adjusted to be as narrow as the fabrication process allows. It would affect the characteristic impedance of the CPW, so it needs to be compensated by adjusting the width of the signal part of the CPW, in order to match the desired impedance, usually 50 Ω.

Given the previous discussion, the proposed concept is shown in Figure 3.1. Initially, the package requires three metal layers (Fig. 3.2), even though the number of layers required would depend on the design of the hosted circuit. Depending on the thickness of the hosted circuit, the dimensions of the CPW ports also need to be adjusted to match the required impedance, as well as the width of the inner feed lines, typically 50 Ω. Parameters h_1 and h_2 are flexible and may be adjusted to match the hosted circuit topology.

3.4 CPW designs

Through the development of the project, several designs have been investigated. For comparison purposes, all of them are designed with the same 0.45 mm thickness ($h_1 = 0.25$ mm, $h_2 = 0.2$ mm) in LCP substrate.

3.4.1 Initial design

As a starting point, a simple design consisting of a CPW section connected to the inner feed lines through a vertical via is evaluated. CPW is designed with the gap as narrow as possible in order to minimize radiation, and its width is chosen to match 50 Ω, for the given 0.45 mm thickness. Width of the feed lines also match 50 Ω as a stripline (Fig. 3.3). Several experiments were carried with this type of launch, including some early versions of the dual-band filters covered in Chapter 4.

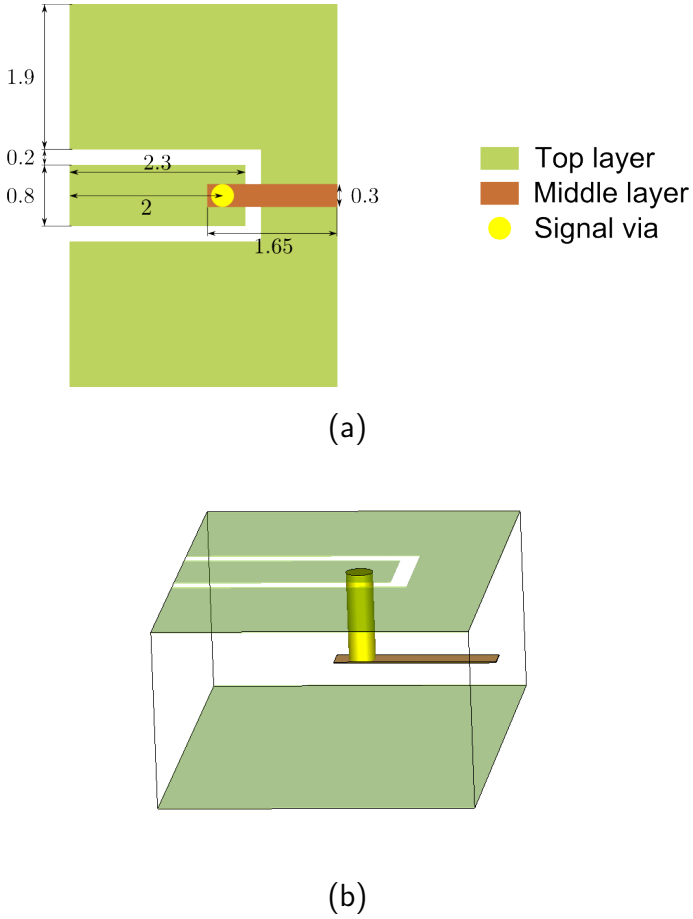
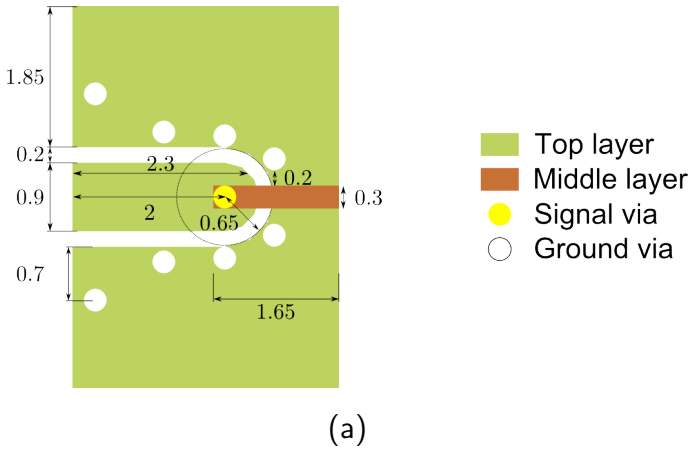


Figure 3.3: First design details. All vias ⌀0.3. Units in mm. (a) 2-D view (b) 3-D view



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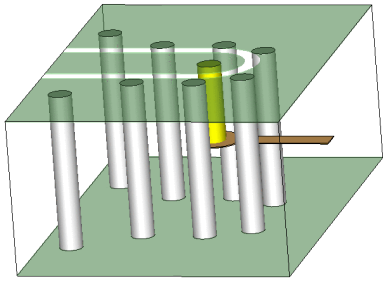


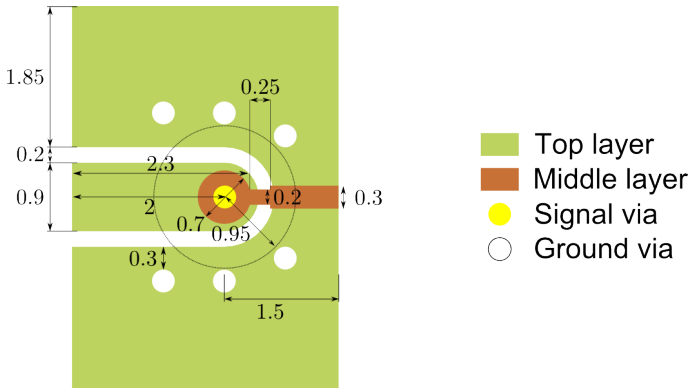
(b)

Figure 3.4: Second design details. All vias ⌀0.3. Units in mm. (a) 2-D view (b) 3-D view

3.4.2 Second design

After some experiments with the initial design, the performance of the launch at higher frequencies was found deficient. The new design focuses on developing a transition where the impedance is better matched to the port impedance throughout the frequency span of interest (0-20 GHz). The idea is to consider the vertical transition as a coaxial transmission line (Fig. 1.2), where the central conductor is the signal via, and some ground vias surrounding it emulating the outer conductor (Fig. 3.4).

Number of vias and its diameter respond to fabrication matters, as increasing the number of vias is associated with fabrication complexity. Taking a 0.3 mm via, the outer conductor diameter that matches 50 Ω, from (1.1), is 1.27 mm. This calculated diameter forces the vias to be placed too close to the CPW gap, reducing the fabrication tolerance. Vias close to the edge (0.7 mm away from CPW) are included based on simulation optimizations.



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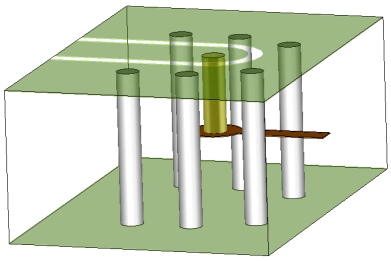


(b)

Figure 3.5: Third design details. All vias ⌀0.3. Units in mm. (a) 2-D view (b) 3-D view

3.4.3 Third design

Third iteration of the packaging solution aims at solving fabrication issues found on the second design, namely ground vias being too close to CPW gap, and misalignment between CPW and feed lines.

Ground vias are moved further from the CPW to allow for more fabrication tolerance (Fig. 3.5). This increases the impedance of the virtual coaxial transition to 64 Ω. In order to address the misalignment issue, the landing point from the CPW is replaced by a circular patch that increases the error margin. From this patch to the actual 50 Ω stripline, a section of higher impedance is placed in order to match the increased impedance of the transition.

3.5 Designs evaluation

In order to evaluate the performance of each launch, all three launches are tested when hosting a 5 mm-long, 50 Ω stripline. The stripline is simulated independently with identical substrate thickness distribution, in order to estimate its losses against frequency from DC to 20 GHz.

3.5.1 Simulations and loss estimation

Full-wave simulations carried on the initial design using CST frequency solver [15], show good matching up to 15 GHz, but then some resonances appear that makes the performance not meet the requirements (Fig. 3.6). The other two designs show similar performances regarding insertion loss, having the latter less ripple due to improved matching. Insertion loss against frequency for these two experiments can be approximated, in dB, by:

$$IL_{EXP}(f) = 0.012f + 0.025 \tag{3.1}$$

with f being the frequency in GHz (Fig. 3.6a).

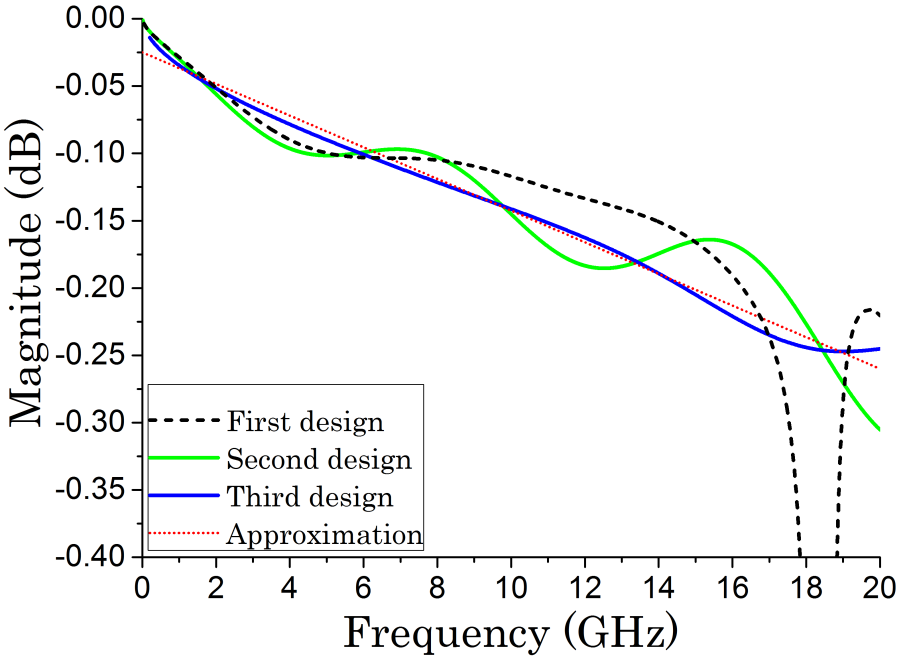
Following a similar approach for the stripline simulation (Fig. 3.7), losses can be approximated by:

$$IL_{SL}(f) = 0.007f + 0.015 \tag{3.2}$$

Furthermore, losses due to the packaging transition can be estimated as the difference between the packaged stripline simulation losses, and the stripline simulation losses, using (3.1) and (3.2). So it can be determined that the losses for each transition are:

$$IL(f) = \frac{IL_{EXP} - IL_{SL}}{2} = \frac{0.005f + 0.01}{2} \tag{3.3}$$

From (3.3), losses at the center of the working bandwidth (10 GHz) are calculated as 0.06 dB.



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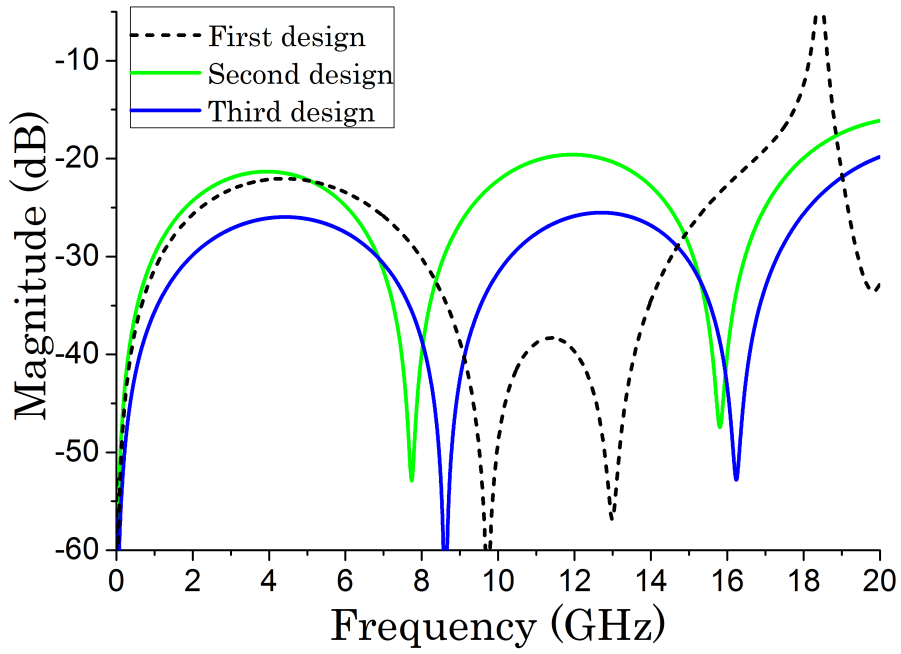

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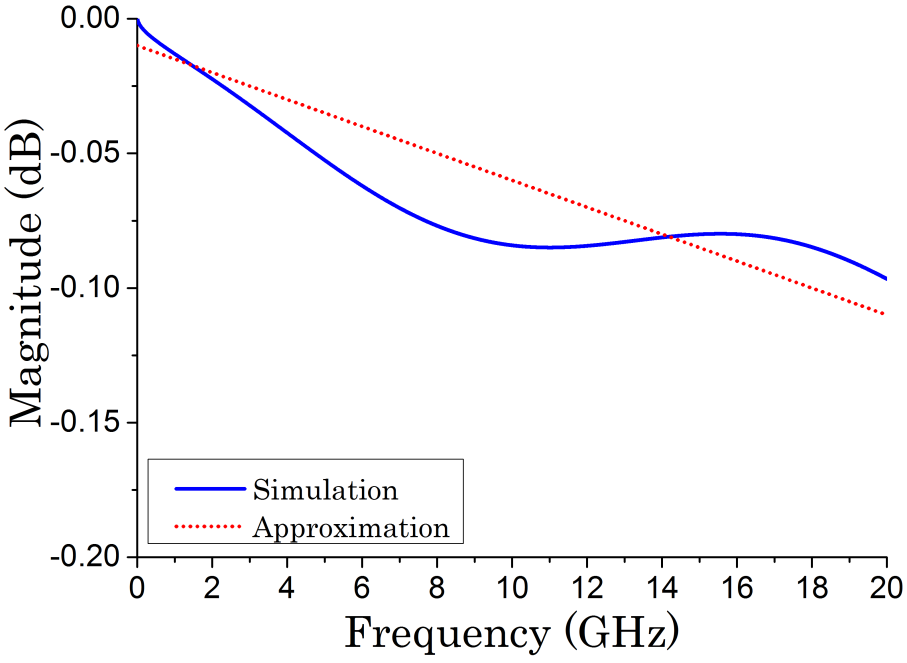
Figure 3.6: Launches full-wave CST simulation comparison (a) Insertion loss (S_{21} magnitude) (b) Return loss (S_{11} magnitude)



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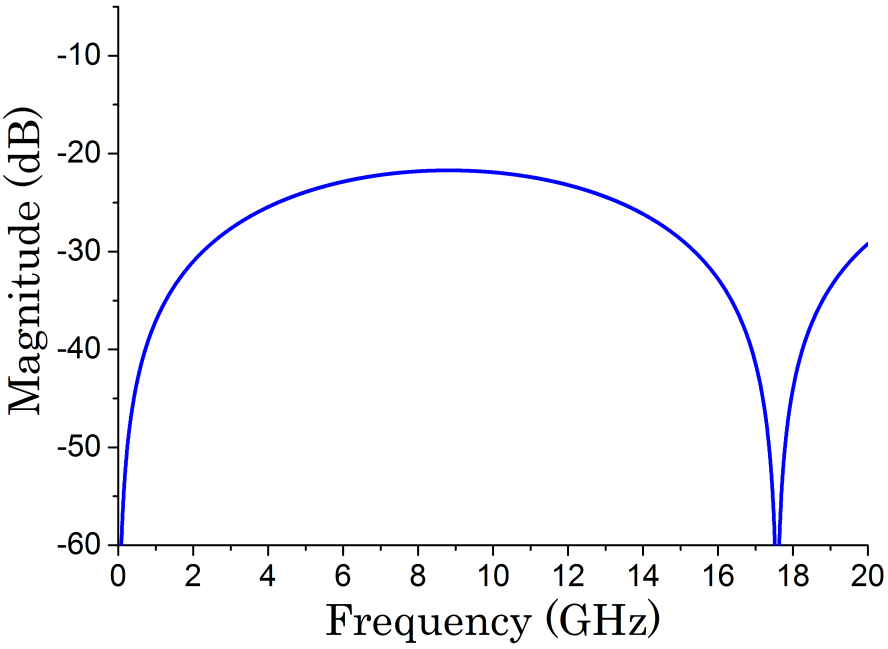


(b)

Figure 3.7: 5 mm-long stripline full-wave CST simulation (a) Insertion loss (S_{21} magnitude) (b) Return loss (S_{11} magnitude)

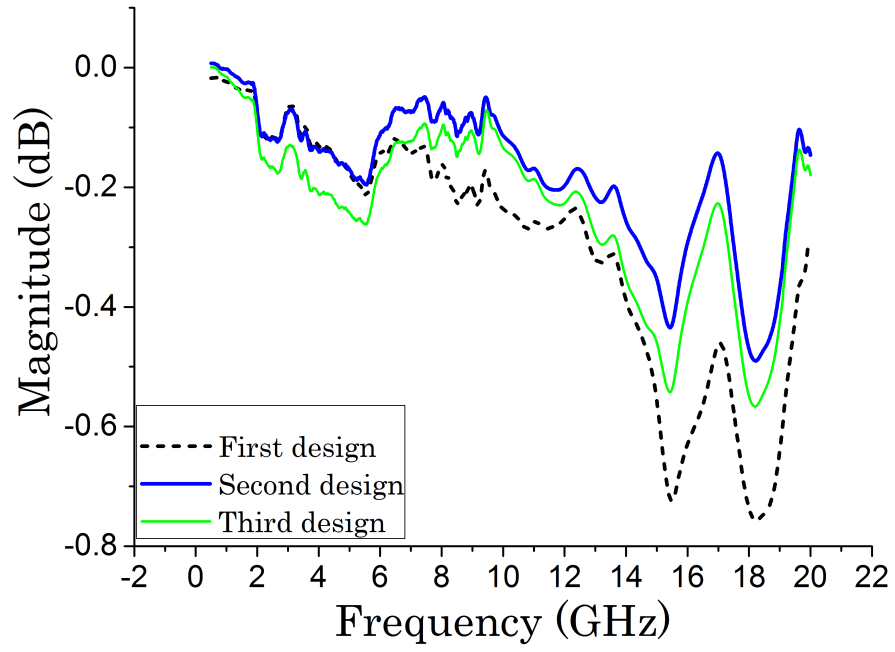
3.5.2 Measured results

Measured results (Fig. 3.8) offer a reasonable agreement with the simulations. All designs show higher losses than predicted in the simulations due to fabrication tolerances, as well as the modelling of the via transitions. However, return loss measurements agree with simulations in terms of what design performs best. First design has better performance at lower frequencies, while the last designs remain stable across the entire frequency span. Out of these two, the third design shows better return loss, apart from the mentioned higher fabrication tolerance.

3.5.3 Fabrication

In order to compare the performances of each design, all three versions of the launch are fabricated in the same experiment, two samples of each, so the comparison is independent from etching or lamination tolerances. Also, designs are distributed alternatively along the fabrication board (Fig. 3.9) to minimize the effects of fabrication errors.

Substrate is comprised of nine layers of LCP (Fig. 3.10) with a total thickness of 0.45 mm. Process described in Chapter 2 is followed. During the fabrication, some problems were found with one of the two samples of the second design, as ground vias were short-circuited with the signal path. This fact reinforces the need for this design to be modified to simplify the fabrication process.



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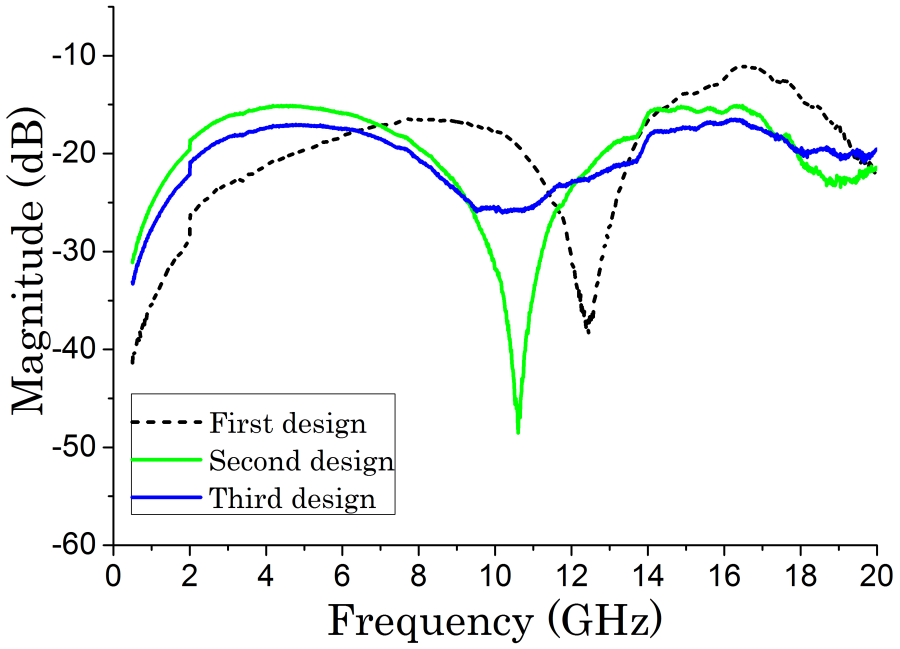

(b)

Figure 3.8: Measurements comparison for the different designs (a) Insertion loss (S_{21} magnitude) (b) Return loss (S_{11} magnitude)

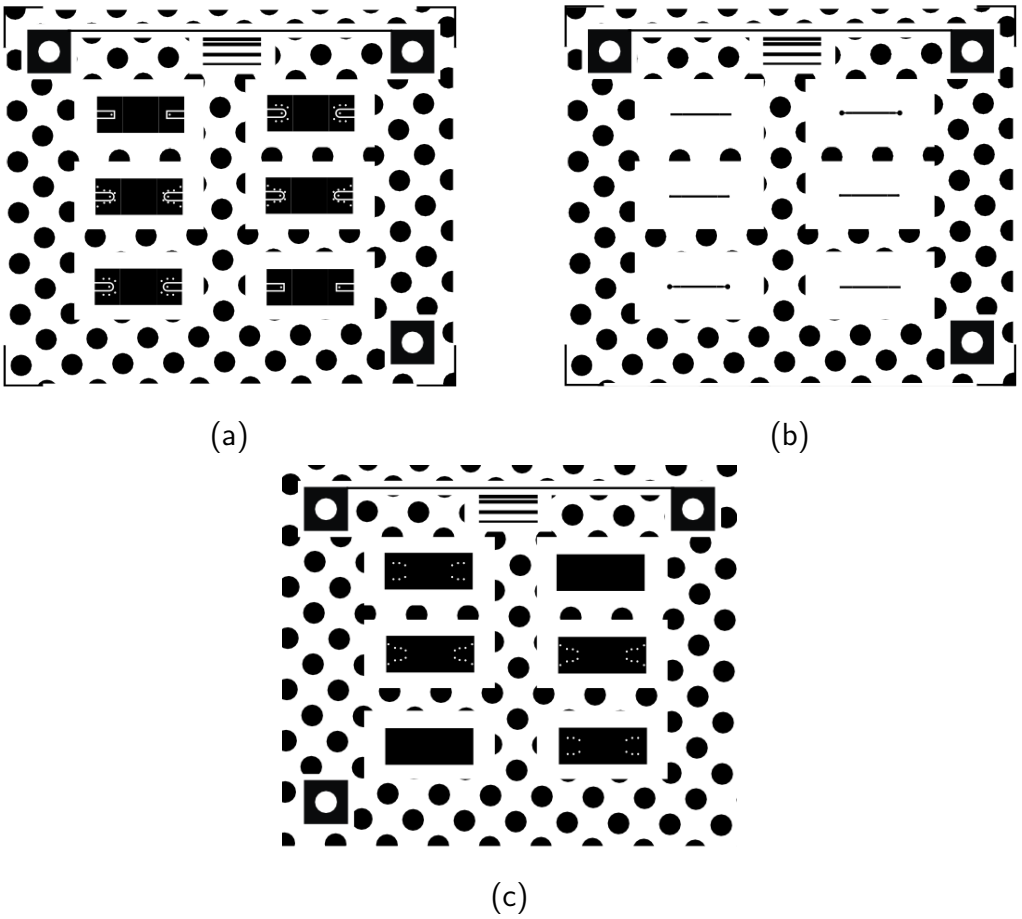

Figure 3.9: Mask for experiment fabrication. (a) CPW layer (b) Stripline layer (c) Ground layer

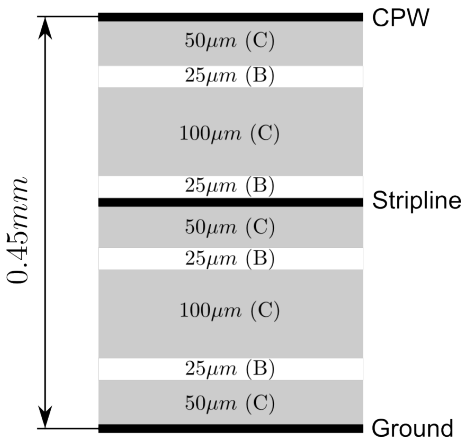

Figure 3.10: Layer distribution for experiment fabrication. (C=Core film, B=Bonding film)

3.6 Conclusions and future work

Along this chapter, a method for producing self-packaged planar filters is studied. The proposed packaging approach integrates with the filter design and fabrication, eliminating the need for including an external box.

Several designs have been presented and fabricated, analysing their performances. Losses introduced to the hosted device are comparable to those of pre-fabricated metal boxes, with the advantage of being this method lighter and more compact. Apart from the experiments described along this chapter, the performance of this packaging system is validated in following chapters, using real filters.

It has been demonstrated how this approach introduces low losses. However, the use of conductive paste on the side walls to provide electromagnetic isolation still must be validated. Furthermore, its isolation level will have to be compared to that of a row of ground vias, as well as an analysis of what method is more convenient for mass production in an industrial environment.

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Chapter 4

Dual band filter

4.1 Introduction

As wireless communications penetrate more and more in our daily lives different systems and transmission technologies have to be developed to fit them properly. Mobile phones or laptops, as an example, often integrate technologies like WiFi, Bluetooth, GSM or GPS. Each of these services has receivers/transmitters operating in different frequencies that have to be accommodated in a small, portable device. Multiband radio frontends are often employed for this matter and here multiband filters play a key role.

Extensive work has been carried recently in the field of dual-band filters [1–14] and different approaches on how to produce the pass-bands have been reported. The most common approach is to employ multimode resonators and locate the passbands at the resonant frequencies [2,3,5–7,11,12]. The resonant modes are split by means of inter-resonator coupling in order to control the bandwidth. The separation between the bands depends on the modes of the resonator, placing some design constraints. Alternatively, in [10] only one ring resonator is used to produce the two passbands. In this case the split of each resonant mode is obtained by a pair of open-circuited stubs attached to the resonator. Even though it has the advantage of using only one resonator, it also has the limitations of a small frequency ratio between the passbands. In the other hand, the use of four resonators is reported in [8, 9]

Additionally, methods for producing each band independently, combining two band-

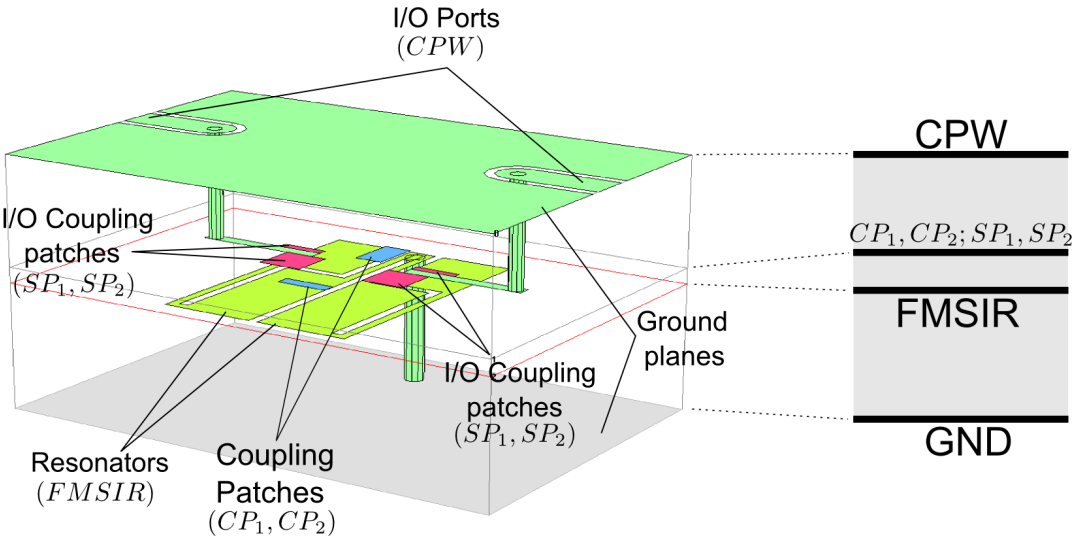


Figure 4.1: Proposed self-packaged dual-band filter multilayer structure

pass filters, have been covered in [4, 14]. Finally, a method based on successive transformations from a lowpass prototype is presented in [1], and a semi-lumped element approach cascading several bandpass cells in reported in [13]. These methods simplify the design process usually at the cost of increased footprint.

The approach followed in this work is the use of a pair of novel multi-mode resonators that extend the concept of stepped-impedance resonators to form the two passbands, providing convenient methods for inter-resonator coupling, and source coupling. Design concept is covered in Section 4.2, followed by a detailed discussion of each design element in subsequent sections. With all the design elements in place, Section 4.7 proposes a method for designing a dual-band filter based on the proposed concept. This method is followed to design two different filters, covered in Sections 4.8 and 4.9. Lastly, conclusions are presented in Section 4.11.

4.2 Design concept

Design of a bandpass filter requires three basic elements: design of the resonator or resonators, which will determine the location of the passband or passbands; adjusting the inter-resonator coupling (k) to determine the bandwidth; and the coupling between the ports and the input/output resonators (Q_e). These elements will be covered in the next sections. In the case of a dual-band filter, these concepts may be applied independently to each band, provided each element can be tuned inde-

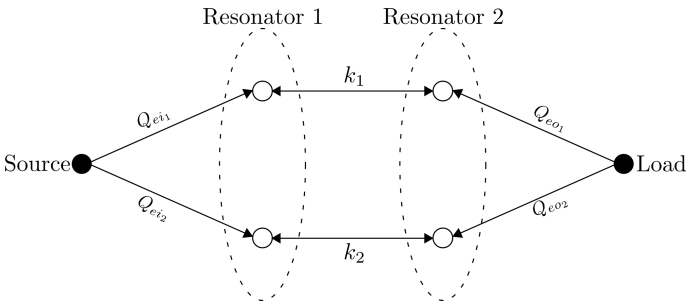


Figure 4.2: Dual band filter model

pendently for each band.

The proposed concept uses two identical multi-mode resonators, from which their first two resonant modes are used to determine the center frequency of each of the two passbands. These are represented by white circles in Fig. 4.2. In the figure, the upper path represents the first passband, and the lower path, the second passband. Each resonant mode is coupled to its equivalent in the twin resonator in order to tune the bandwidth (k_1, k_2). Finally, each resonant mode needs to be coupled to the source (Q_{ei_1}, Q_{ei_2}) and load (Q_{eo_1}, Q_{eo_2}), represented by black circles.

The multilayer structure proposed in this work (Fig. 4.1) is distributed in two metal layers. On the lower layer, two multi-mode resonators are placed next to each other in a mirrored disposition. Inter-resonator coupling is produced, firstly, by the proximity between them and, secondly, by a pair of metal patches (CP_1, CP_2), placed on the layer above them. These patches control both k_1 and k_2. Finally, the coupling between the resonators and the source/load ports is achieved by a second pair of patches (SP_1, SP_2) which area determines Q_{ei} and Q_{eo} for each band. The filter is contained within two ground planes in order to produce a self-packaged filter, as described in Chapter 3.

Design of bandpass filters are usually based on a low-pass filter prototype and then a bandpass transformation is applied to obtain the correspondent design parameters. In this case, the design is based on a lowpass, second-order Chebyshev prototype (Fig. 4.3). Since each band has its own k and Q_e, the low-pass prototype transformation can be applied separately to each band. Bandpass transformation results in the following design equations [15]:

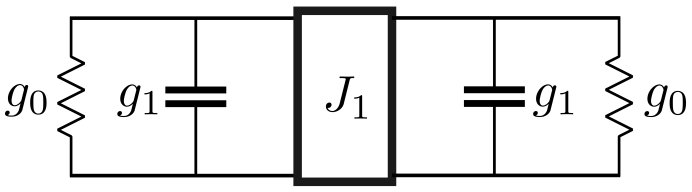


Figure 4.3: Lowpass prototype filter

$$Q_{ei_1} = Q_{eo_1} = \frac{g_1}{FBW_1} \qquad Q_{ei_2} = Q_{eo_2} = \frac{g_1}{FBW_2} \tag{4.1}$$

$$k_1 = \frac{FBW_1 J_1}{g_1} \qquad k_2 = \frac{FBW_2 J_1}{g_1} \tag{4.2}$$

where Q_{ei_n} and Q_{eo_n} are the input and output external quality factors, k_n is the coupling coefficient, and FBW_n is the fractional ripple bandwidth. Index n represents the band. Values for g_0, g_1, and J_1 are calculated for the prototype based on the required order of the filter and the required return loss.

4.3 Multi-mode resonator

Resonators are a key element when designing bandpass filters. For this work a new type of multi-mode resonator has been developed by extending the stepped-impedance resonator concept. In this section, different types of quarter-wavelength resonators are introduced, beginning with an uniform impedance line, followed by single-stepped-impedance resonators, concluding with the proposed folded multi-stepped impedance resonator (FMSIR), and the advantages it introduces over the former. Note all these three types have one shorted-to-ground end so they act as a quarter-wavelength resonator. If both ends were left open, they would behave as a half-wavelength resonator, requiring double the physical length to produce a resonance at the same frequency as a quarter-wavelength.

4.3.1 Uniform quarter-wavelength resonators

A section of transmission line with uniform characteristic impedance, and one of its ends short-circuited (Fig. 4.4), is known as conventional quarter-wavelength

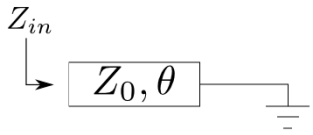


Figure 4.4: 1/4 wavelength uniform impedance resonator model

resonator (UIR). Looking at the resonator from the open-end terminal, the input impedance is:

$$Z_{in} = jZ_0 \tan(\theta) \tag{4.3}$$

The condition for resonance is $Z_{in} = \infty$, leading to resonances at $\theta = (2n+1)\frac{\pi}{2}$ with $n = 1, 2, 3....$ Furthermore, the guided wavelength (λ) can be approximated [15] as:

$$\lambda = \frac{300}{f(GHz)\sqrt{\epsilon_{er}}} \tag{4.4}$$

where ϵ_{er} is the effective dielectric constant. Since, by definition:

$$\theta = \beta l \tag{4.5}$$

$$\beta = \frac{2\pi}{\lambda} \tag{4.6}$$

expression (4.4) can be rewritten, in terms of frequency, as:

$$f_n(GHz) = \frac{300}{(2n+1)\frac{l(mm)}{4}\sqrt{\epsilon_{er}}} \tag{4.7}$$

where n represents the order of the harmonic, with f_0 being the fundamental resonant frequency, and l is the physical length of the resonator.

4.3.2 Stepped-impedance quarter-wavelength resonator

A quarter-wavelength stepped-impedance resonator (SIR) is a variation of the UIR, formed by two sections with different characteristic impedance, while still keeping

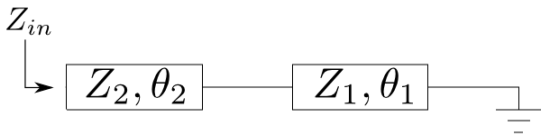


Figure 4.5: 1/4 wavelength stepped impedance resonator model

one of the ends short-circuited (Fig. 4.5). In this case, the input impedance is found as:

$$Z_{in} = jR_Z \frac{\tan(\theta_1) + R_Z \tan(\theta_2)}{R_Z - \tan(\theta_1)\tan(\theta_2)} \tag{4.8}$$

Where $R_Z = \frac{Z_2}{Z_1}$ is the impedance ratio, and θ_1 and θ_2 are the electrical lengths of each section. From that, the resonance condition is:

$$R_Z = \tan(\theta_1)\tan(\theta_2) \tag{4.9}$$

It can be noted how the resonant condition is affected by R_Z and the electrical lengths θ_1 and θ_2. For convenience, let R_θ be defined as the electrical length ratio:

$$R_\theta = \frac{\theta_2}{\theta_1} \tag{4.10}$$

In order to determine the harmonic resonances, R_Z is the most relevant parameter, even though R_θ also has an impact, specially for lower values of R_Z (Fig. 4.6). Note how $R_\theta = 0.5$ and $R_\theta = 2$ are equivalent cases, and $R_\theta = 0$ and $R_\theta = \infty$ correspond to the UIR case. The main advantage introduced by SIR over UIR is the ability to control the ratio of the harmonic resonant modes.

For comparison, and following the procedure described in [16], the normalized length (L_n) of the SIR in respect of that of a conventional UIR is defined as:

$$L_n = \frac{\theta_T}{\pi/2} = \frac{\theta_1 + \theta_2}{\pi/2} \tag{4.11}$$

From (4.9) and (4.11), we obtain:

$$L_n = \frac{\theta_1 + \tan^{-1}\frac{R_Z}{\tan\theta_1}}{\pi/2} \tag{4.12}$$

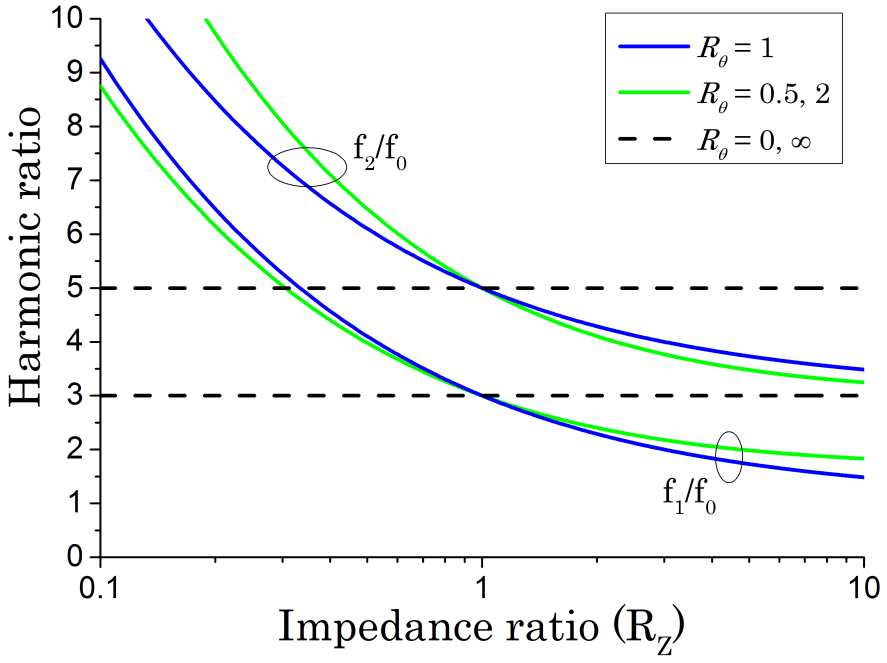


Figure 4.6: SIR length ratio and first two harmonics

From this relationship it is concluded that for values of $R_Z < 1$, the same fundamental frequency as in a UIR is obtained with a shorter SIR, while for $R_Z > 1$ the resultant SIR is larger than its UIR counterpart (Fig. 4.7).

4.3.3 Folded multi-stepped impedance resonator

For this work, a folded multi-stepped impedance resonator (FMSIR) has been developed. It consists of four sections alternating high- and low-impedance, with one end open- and the other end short-circuited, as a quarter-wavelength resonator (Fig. 4.8). This alternating structure allows for a compact layout when folding two sections over the other two. The input impedance (Z_{in}), looking into the open end of the resonator, can be determined as:

$$Z_{in} = \frac{jZ_1R_Z(1+R_Z)}{\Delta}\left(R_Z\frac{(\tan\theta_1+\tan\theta_2)^2}{\tan(\theta_1+\theta_2)} - (R_Z-1)^2\tan\theta_1\tan^2\theta_2)\right) \tag{4.13}$$

$$\Delta = (R_Z - \tan\theta_1\tan\theta_2)^2 - R_Z(\tan\theta_1 + R_Z\tan\theta_2)^2$$

with $R_Z = Z_2/Z_1$ defined as the impedance ratio between the lines. From (4.13) the resonance condition is described as:

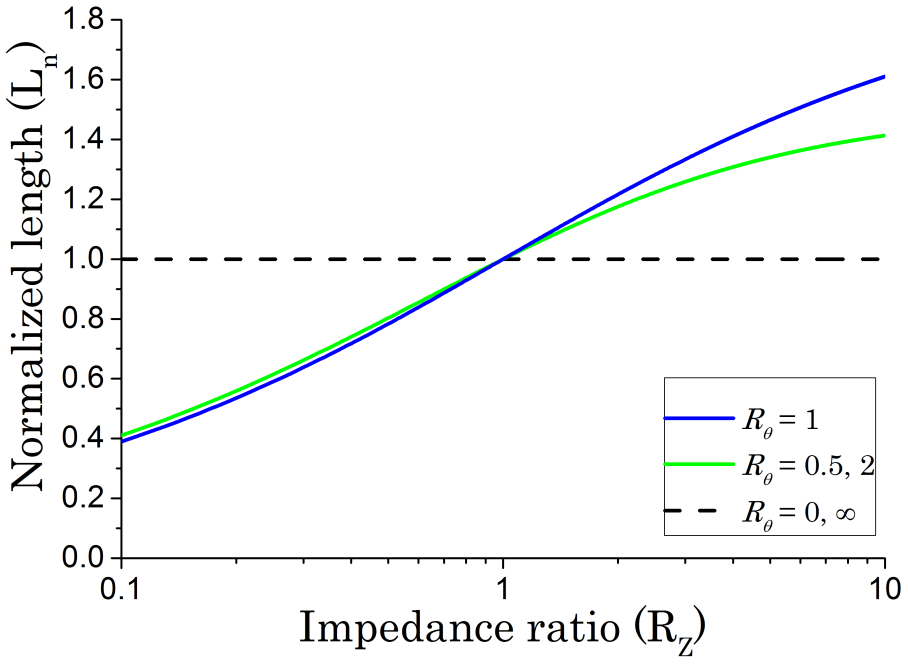


Figure 4.7: SIR normalized length in respect of that of a UIR for different values of R_θ and R_Z. Equivalent to the ratio between fundamental resonant frequencies when both lengths are equal.

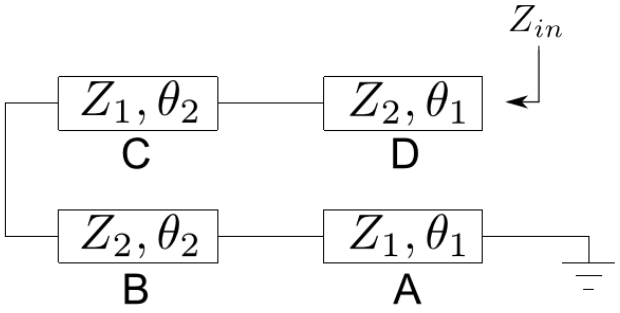


Figure 4.8: FMSIR transmission line model. Letter A-D denoting individual line sections

$$(R_Z - \tan\theta_1 \tan\theta_2)^2 = R_Z(\tan\theta_1 + R_Z \tan\theta_2)^2 \tag{4.14}$$

By defining the line length ratio as $R_\theta = \theta_2/\theta_1$, the resonators behavior can be fully determined according to R_Z, R_θ. From (4.14) it can be appreciated how R_θ has a higher impact on the harmonic configuration than in the SIR case (Fig. 4.9). Note the special cases $R_\theta = 0$ and $R_\theta = \infty$, equivalent to the case of a SIR with $R_\theta = 1$ and same R_Z in the former, and inverted R_Z in the latter.

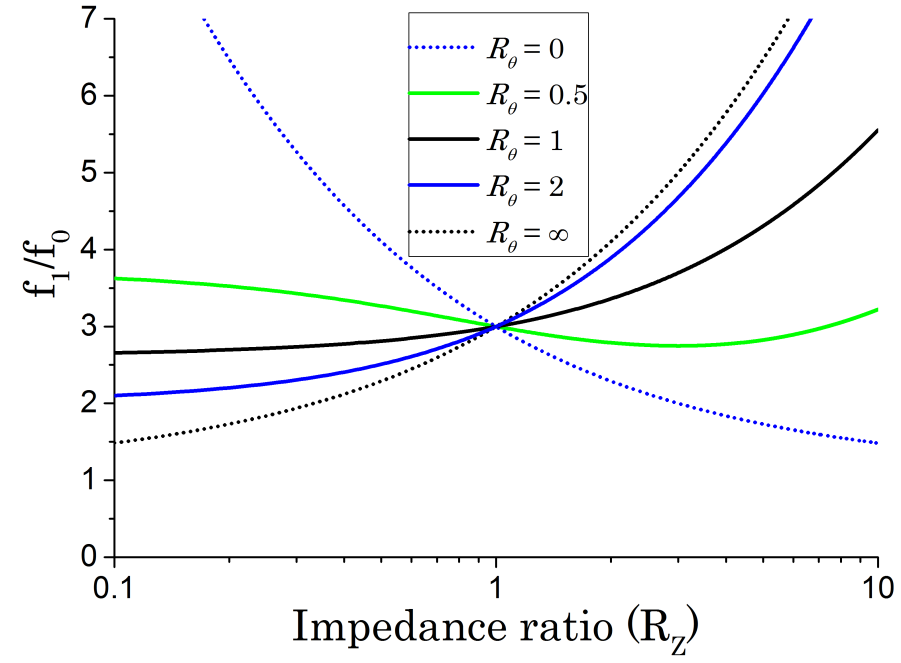
Similarly to SIR, this type of resonator has the advantage of controlling the first harmonic with R_Z and R_θ. However, it also has the interesting advantage of pushing the second harmonic to higher frequencies, enabling the possibility of producing wider stopbands when applied to a bandpass filter. Additionally, for values of $R_Z < 1$, the first harmonic is almost constant regardless of R_Z. This fact increases the fabrication tolerance, specially when working with chemical etching, as it introduces errors to the width of the lines.

Following the comparison to UIR, L_n is defined for the FMSIR as:

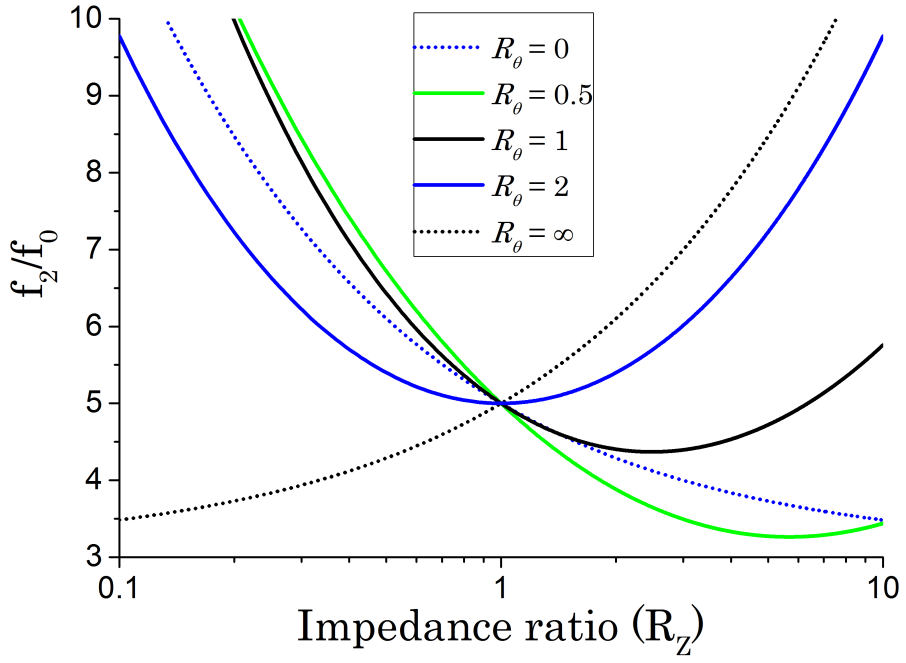
$$L_n = \frac{\theta_T}{\pi/2} = \frac{2(\theta_1 + \theta_2)}{\pi/2} = \frac{2(1 + R_\theta)\theta_1}{\pi/2} \tag{4.15}$$

Values from (4.15) are plotted in Fig. 4.10. It can be seen how this type of resonator is smaller than an UIR for the same resonant frequency, for values of $R_Z < 1$. Furthermore, for $R_Z > 1$ the size is larger in some cases, but still smaller in most cases, and always shorter than a SIR.

FMSIR provides highest footprint reduction when two of its sections are folded over the other two (Fig. 4.11). With this configuration, spurious coupling is expected between adjacent lines, being stronger where the current density is higher and the distance between them, smaller. However, at resonant frequencies, most of the current density is accumulated at the high-impedance sections, which are always next to a low-impedance section, with low current density (Fig. 4.12). This property makes the coupling between adjacent lines negligible. Therefore, it is convenient to keep the gap to a minimum in order to approximate the dimensions to the ideal model ($\Delta_L = 0$).



(a)



(b)

Figure 4.9: FMSIR harmonics for different values of R_θ and R_Z (a) First harmonic (f_1/f_0) (b) Second harmonic (f_2/f_0)

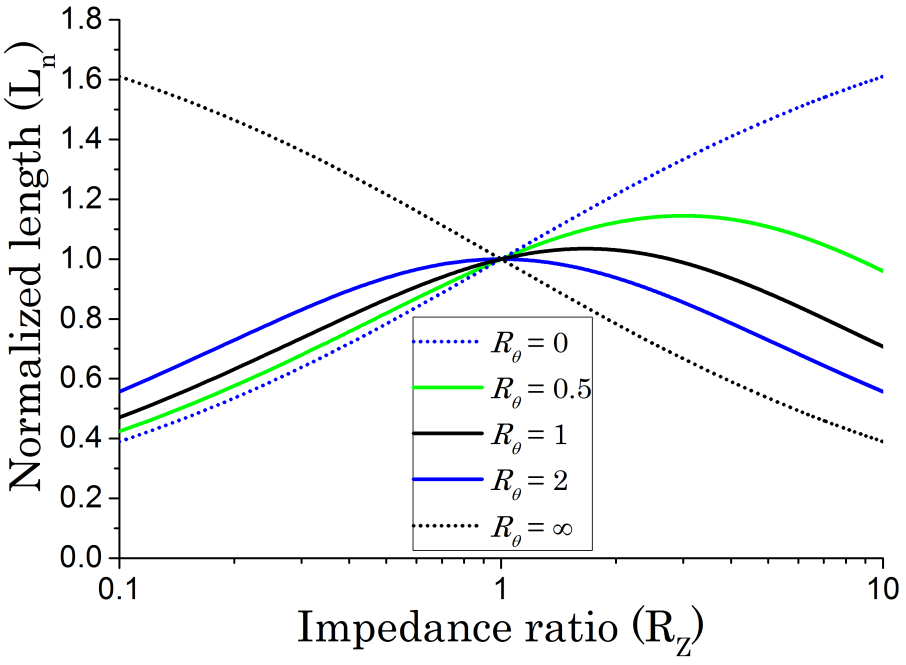


Figure 4.10: FMSIR normalized length in respect of that of a UIR for different values of R_θ and R_Z. Equivalent to the ratio between fundamental resonant frequencies when both lengths are equal.

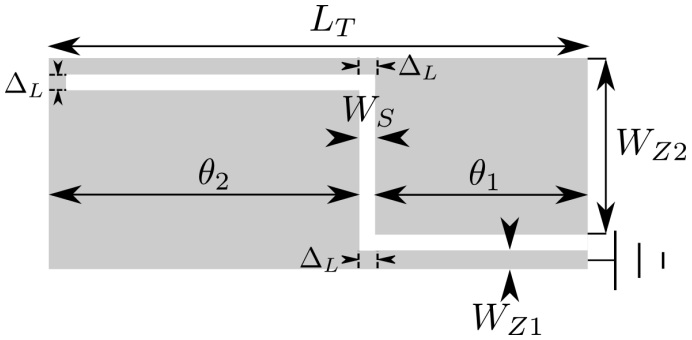


Figure 4.11: FMSIR proposed layout

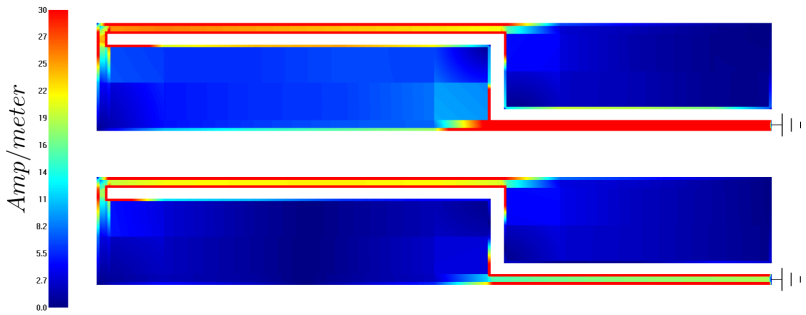


Figure 4.12: Current density distribution example for the first two resonant modes. Top: fundamental resonant mode. Bottom: first harmonic.

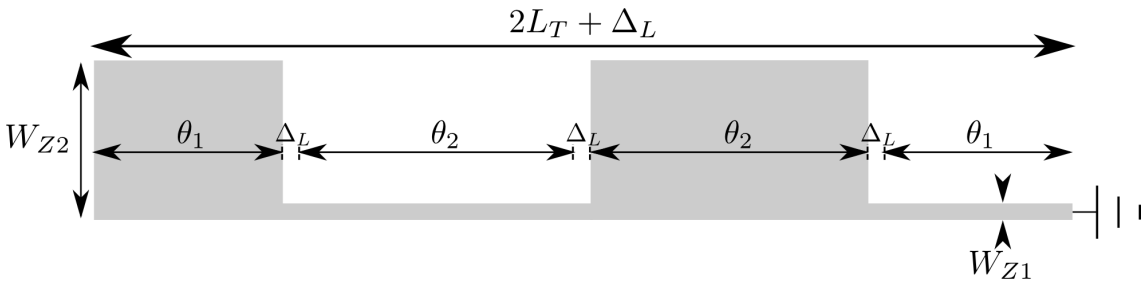


Figure 4.13: Unfolded MSIR layout

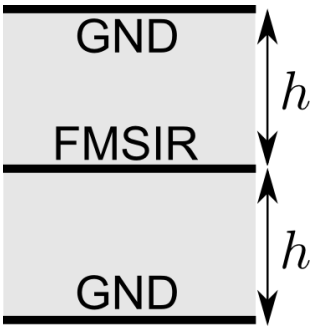


Figure 4.14: Resonator layer distribution

Furthermore, unfolding the FMSIR would result in a resonator version with expanded A and C sections (Fig. 4.13), compared to the ideal model (Fig. 4.8). Full EM simulation of both resonators, FMSIR and unfolded, under the same conditions of LCP substrate (Fig. 4.14) and dimensions (Table 4.1), demonstrates there is little variation on the resonators' responses (Fig. 4.15). A summary of the simulated resonating frequencies is shown in Table 4.2.

θ_1	5 mm
θ_2	7.35 mm
Δ_L	0.2 mm

W_{Z1}	0.2 mm
W_{Z2}	1.6 mm
h	0.2 mm

Table 4.1: Dimension parameters used for comparison

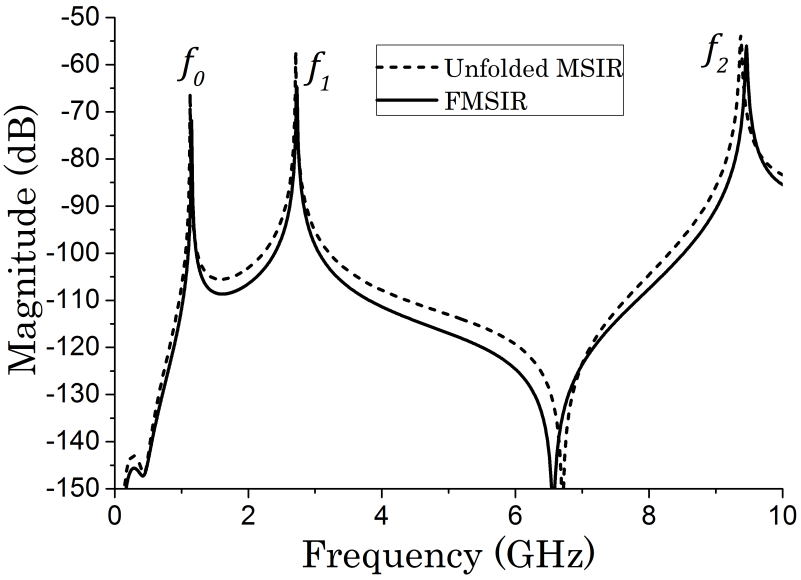


Figure 4.15: FMSIR vs. Unfolded MSIR resonant modes comparison

	f_0	f_1	f_2
FMSIR	1.15 GHz	2.73 GHz	9.46 GHz
Unfolded	1.13 GHz	2.71 GHz	9.37 GHz

Table 4.2: FMSIR vs. Unfolded MSIR. Resonant frequencies in GHz

4.4 External quality factor

In a resonant circuit, a parameter of great importance is the quality factor (Q), as it has a big influence on how sharp the transition from passband to stopband is. Q is defined as [17]:

$$Q = \omega \frac{energy_stored}{energy_loss/second} \tag{4.16}$$

where ω is the angular resonant frequency. This definition applies to a resonant structure on its own, in the absence of any loading effects caused by other elements in the circuit. Other elements in the circuit will decrease Q, so a loaded quality factor Q_L may be defined as:

$$\frac{1}{Q_L} = \frac{1}{Q} + \frac{1}{Q_e} \tag{4.17}$$

where Q_e is the so-called external quality factor, as a measurement of how external circuitry affects the resonator's Q_L. In the case of this study, Q_e will be determined

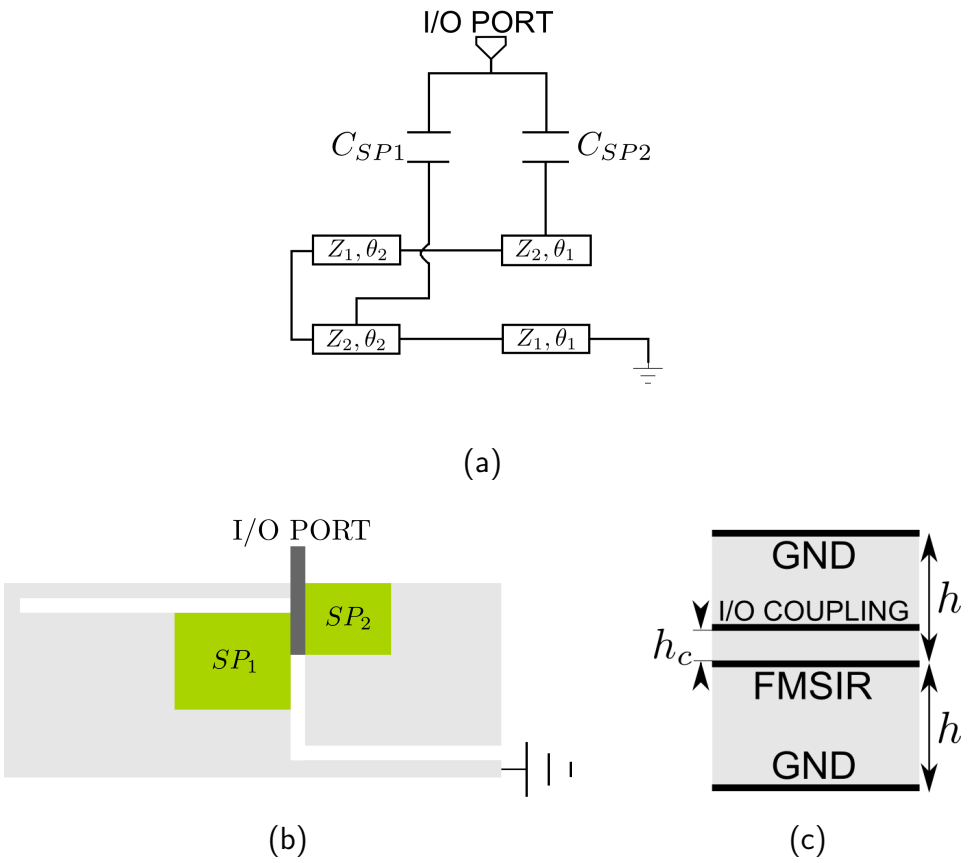


Figure 4.16: I/O coupling (a) Simplified transmission line model. (b) Physical realization (top view) (c) Layer distribution

by the amount of coupling between source/load and a resonator. Higher coupling implies lower Q_e.

The resonator is coupled to the source through a pair of capacitances (C_{SP1},C_{SP2}) created between the low-impedance sections of the resonator and the port (Fig. 4.16a). These capacitances are created by means of a pair of metal patches placed, on a different layer, above the low-impedance sections of the resonator (SP_1, SP_2) (Fig. 4.16b). The amount of coupling is determined by the amount of capacitance created between the metal patches, as a parallel-plates capacitor. As the capacitance is increased, Q_e decreases. It is important to note that the modelling the load as a capacitance is only valid for low frequencies. The actual value of the capacitance created between the patches and the resonator will grow as frequency is increased until the capacitor's self-resonant frequency is reached.

In general, increasing the size of the patches will increase the coupling and hence reduce the external quality factor (Q_e). However, the variation of each patch will affect both bands, meaning the value of the (Q_{e1}, Q_{e2}) set is a function of both

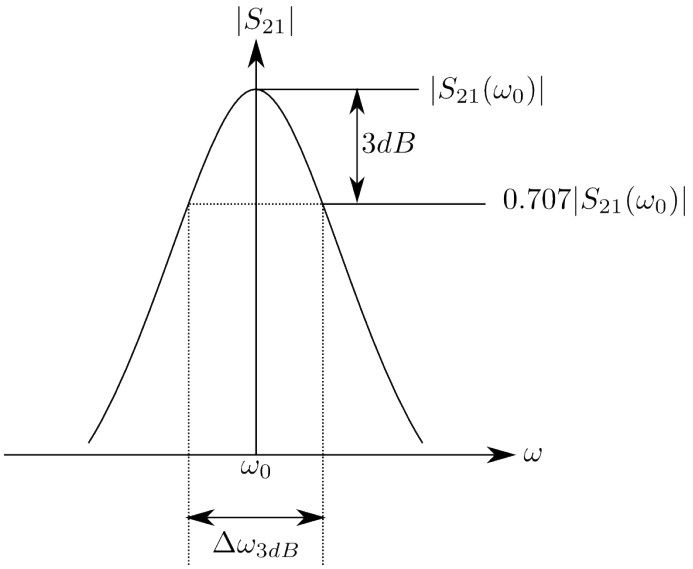


Figure 4.17: Response from weakly excited loaded resonator

coupling patches, i.e. SP_1 and SP_2 (refer to Figs. 4.20, 4.24). Q_e is extracted using a technique described in [15].

When loading the FMSIR with C_{SP1} and C_{SP2}, a shift of the resonant modes towards lower frequencies is expected.

4.4.1 External quality factor extraction

The method for extracting this parameter from full EM simulations is described in [15]. By weakly exciting a resonator coupled to a source, the resonant frequency can be found from the peak response $|S_{21}(\omega_0)|$ (Fig. 4.17). Then Q_e can be found from the center frequency and the difference between the 3-dB cutoff points:

$$Q_e = \frac{\omega_0}{\Delta\omega_{3dB}} \tag{4.18}$$

4.5 Inter-resonator coupling

It is well known when microwave resonators are in proximity of each other, the interaction of their magnetic and electric fields modify their resonant frequency. This property has been covered in several studies [15, 18, 19], both including interaction between resonators with the same resonant frequency (synchronously tuned) or with

different resonant frequencies (asynchronously tuned). The amount of interaction between the resonators is known as the inter-resonator coupling coefficient (k).

In the case of synchronously tuned resonators this interaction shifts each resonator's frequency away from its natural resonance, resulting in two resonant frequencies instead of one, in the vicinity of the resonators' resonant frequency. The higher k is, the wider the spacing between the resultant resonant frequencies. This property is particularly interesting when applied to narrow passband filters, as these two, or more, resonant frequencies may form a passband under certain conditions.

In order to produce the two desired passbands for the proposed filter, proper couplings need to be facilitated. This is achieved by two different means: firstly, the proximity of the resonators on the same layer, as previously discussed; and secondly by two metal patches (CP_1, CP_2) placed on the layer above the resonators along the symmetry plane. These two patches allow for higher control over k by introducing a capacitance between the resonators that further modifies the electrical field between them, hence affecting k. The individual equivalent patches for each resonator are joined together to form one single piece of metal (Fig. 4.18b).

The coupling coefficient of coupled microwave resonators may be defined on the basis of a ratio of coupled to stored energy [15]. This coupling coefficient (k) between the resonators may be electric (or capacitive) or magnetic (or inductive), being always a mix of both with one of them being dominant. To determine the k between two resonators the circuit is simulated by separately inserting a magnetic and an electric wall in the plane of symmetry between both resonators. These two separate experiments allow to independently measure the resonant frequency produced by the electric and the magnetic component of k, f_e and f_m, for electric and magnetic wall, respectively. From [18, 19] it can be found that if $f_e > f_m$ the coupling is predominantly magnetic and if $f_e < f_m$ it is predominantly electric. The effective k is calculated by:

$$k = \frac{f_e^2 - f_m^2}{f_e^2 + f_m^2} \tag{4.19}$$

The coupling produced by the proximity of the resonators is predominantly magnetic and is stronger as the separation (GAP) is reduced. Fabrication tolerances place a limitation in the amount of coupling that can be obtained. Furthermore, by solely

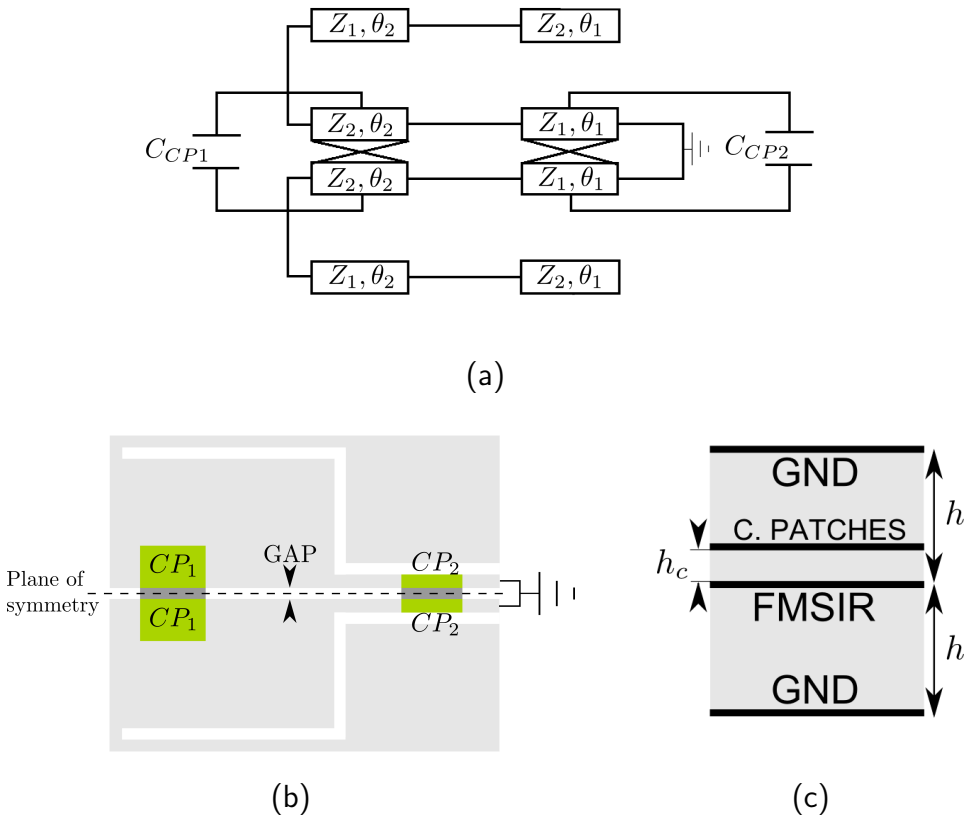


Figure 4.18: Inter-resonator coupling (a) Simplified transmission line model, including optional C_{TZ} (b) Physical realization (top view) (c) Layer distribution

modifying the gap it is not possible to control k independently for each band.

Independent control over the coupling of each band separately (k_1, k_2) comes from the coupling patches CP_1 and CP_2. These two patches create the capacitances C_{CP1} and C_{CP2}, respectively (Fig. 4.18a) contributing to k_1 and k_2 differently. This property makes tuning k for each band possible. The type of coupling they produce is also different due to their positioning on the symmetry line. From Figure 4.12 it is seen how the current density is higher in the high-impedance sections, and minimum at the other end of the symmetry line. Coupling between the high-density current sections, with high inductance, contribute towards magnetic (inductive) coupling, and low-density current sections, predominantly capacitive, towards electric (capacitive) coupling. Hence, by placing CP_1 at the left end of the symmetry line it will be adding electric coupling, in different amount, to k_1 and k_2. As the position of CP_1 is shifted towards the other end, its contribution to the coupling progressively turns into magnetic. Similarly, from CP_2 the contribution is initially magnetic when placed at the rightmost of the symmetry line, turning into electric as shifted away from that point.

In general, the coupling will be stronger as their area of CP_1 and CP_2 is increased. However, since the effective k is a mix of both types of coupling, it could happen that they cancel each other when electric and magnetic coupling are equally strong. Getting the desired k_1 and k_2 is a combination of tuning GAP, areas of CP_1 and CP_2 and their position along the symmetry line.

4.6 Transmission zeros mechanism of generation

Inclusion of additional transmission zeros (TZ) is desirable as it can contribute to increase the selectivity of the passbands and the inter-band rejection. In this design, several TZs are excited due to the different resonating modes of the FMSIR. A low frequency TZ is generated by the resonance of the SIR formed by the transmission line sections C and D (Fig. 4.8). This mode is excited when section B acts as a virtual connection to ground, making the aforementioned sections C and D behave as a $\lambda/4$ SIR. This mode will typically show between the two passbands. Moreover, a second resonant mode from this structure is also excited in the stopband. The frequencies for these modes can be calculated using the equations for SIR found in [16]. These two TZs are split into two pairs when inter-resonator coupling is put in place, and further control over them can be made by specifically coupling the sections C and D of both resonator. In this case, this is achieved by adding the capacitor C_{TZ} (Fig. 4.19).

Depending on the position of the pair SP_1 and SP_2, two modes are excited. From the I/O patches looking into sections B and C, the resultant section behaves as an open-ended UIR with length θ_2. This section anti-resonates at odd multiples of $\lambda/4$.

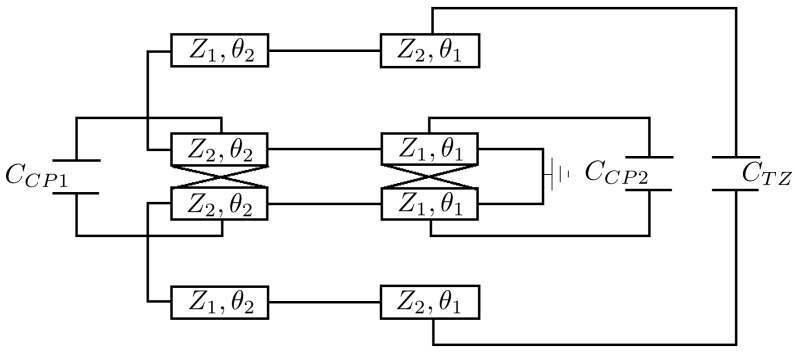


Figure 4.19: Inter-resonator coupling with additional transmission zero

As previously discussed, the inter-resonator coupling is also able to split this TZ in two.

4.7 Design procedure

Due to the structure being so compact, the designs of resonator, I/O coupling and inter-resonator coupling are not really independent. Nevertheless, the design procedure described below can be useful:

- Depending on the selected substrate's dielectric constant and thickness, estimate a value for R_Z that is feasible and provides enough fabrication tolerance.
- Find R_θ that satisfies the required harmonic separation with the help of Fig. 4.9 for the chosen R_Z.
- Calculate the length for a UIR for the required fundamental frequency, as a reference for the FMSIR, using:

$$L_{UIR} = \frac{\lambda_g}{4} \approx \frac{1}{4}\frac{300}{f(GHz)\sqrt{\epsilon_r}} \tag{4.20}$$

- Get L_n from Fig. 4.10 for the required R_Z.
- Calculate the physical length of each section of the ideal FMSIR, i.e. without considering Δ_L, using:

$$L = L_n L_{UIR} = 2(L_{\theta 1} + L_{\theta 2}) \tag{4.21}$$

$$L_{\theta 2} = R_\theta L_{\theta 1} \tag{4.22}$$

  where $L_{\theta 1}$ and $L_{\theta 2}$ are the physical lengths of θ_1 and θ_2, respectively, and L is the physical length of the FMSIR's ideal version.

- Fix a value for W_S (see Fig. 4.11 for reference) as little as the fabrication process allows to, so the FMSIR's total length (L_T) can be found as:

$$L_T = \frac{L}{2} + W_S \tag{4.23}$$

- Adjust FMSIR as required in order to compensate for W_S.
- Calculate the required values of Q_e and k for each band using (4.1) and (4.2).
- Determine the size for the source coupling patches SP_1 and SP_2 that match the calculated Q_{e1} and Q_{e2}. A generic method for this calculation cannot be provided as these values depend on the resonator itself. However Fig. 4.20 and Fig. 4.24 can be used for guidance.
- Determine the size for the coupling patches CP_1 and CP_2 that match the calculated k_1 and k_2. Again, a generic method for this calculation cannot be provided, and Fig. 4.21 and Fig. 4.25 should be used as reference.
- Adjust the resonator's dimensions to compensate for the patches.

4.8 Dual band filter 1.2/2.4 GHz passbands

In order to validate the previous analysis and parameter extraction, a design example is introduced in this section. Initial requirements for the design are:

- First passband centered in 1.2 GHz with a 10% fractional bandwidth.
- Second passband centered in 2.4 GHz with a 8% fractional bandwidth.
- Return loss 20 dB.
- Stop band after second passband up to, at least, 8 times the center frequency of the first passband.

It is desirable for the design to have a low profile, thickness of the layers are kept as thin as possible, while providing enough separation between the ground planes to allow for easy control of line's characteristic impedances. In this case, $h = 0.2$mm and $h_c = 0.025$mm (refer to Figs. 4.16c and 4.18c), leading to a total thickness of 0.4 mm.

4.8.1 Design

Design procedure previously described is followed. As a first step, and with the previous considerations regarding the substrate, the highest impedance achievable

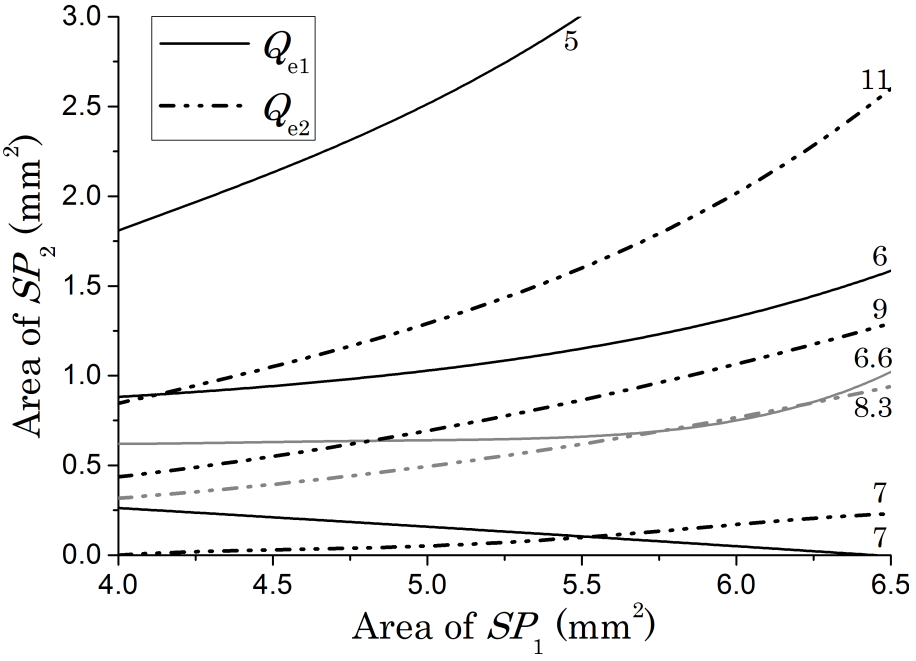


Figure 4.20: 1.2/2.4 GHz design. External quality factor (see Fig. 4.22 for resonator's dimensions). $h_c = 0.025$ mm, $h = 0.2$ mm, $\epsilon_r = 3$.

with available technology is 48 Ω, owing to a 0.2 mm-wide line. Choosing $R_Z = 0.25$, we can establish $Z_1 = 48$ Ω and $Z_2 = 12$ Ω. Low-impedance is obtained with a 1.6 mm-wide line.

In the following steps, R_θ is found as 3.4, and L_{UIR} is calculated for 1.2 GHz, resulting in 36.08 mm. Applying $L_n = 0.8$, the length for the ideal FMSIR (L) is 28.86 mm. From (4.21) and (4.22), $L_{\theta 1}$ and $L_{\theta 2}$ are found as 3.28 mm and 11.15 mm, respectively.

Considering the fabrication limitations, W_S is set to 0.2 mm so, from (4.23), L_T becomes 14.63 mm. In order to compensate for the extra length, and with the help of an EM simulator [20] R_θ needs to be adjusted to 2.9. Additionally, the ground connection for each resonator is shared for simplicity, and A-sections of each resonator are reduced by 0.8 mm, forcing further tuning to the resonator.

For the required return loss of 20 dB, and based on a second order low pass prototype, the required normalized parameters are $g_0 = 1.0$, $g_1 = 0.665$, $J_1 = 0.905$. Then, from (4.1), the values $Q_{e1} = 6.6$ and $Q_{e2} = 8.3$ are obtained. Following the discussion from the previous section, from Fig. 4.20, the point where the curve $Q_{e1} = 6.6$ crosses $Q_{e2} = 8.3$ shows the required values for SP_1 and SP_2: 6 mm^2 and 0.7

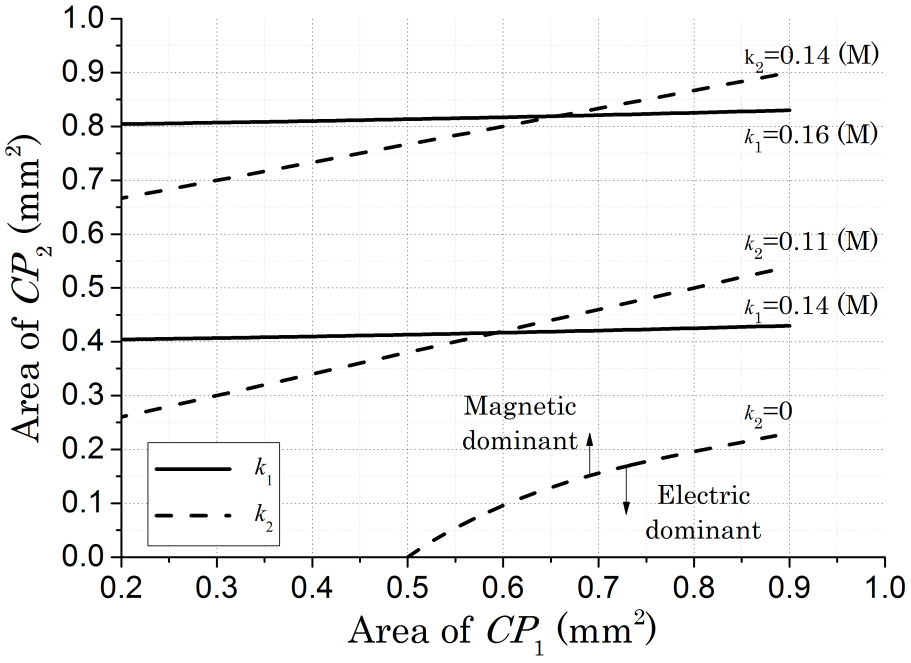
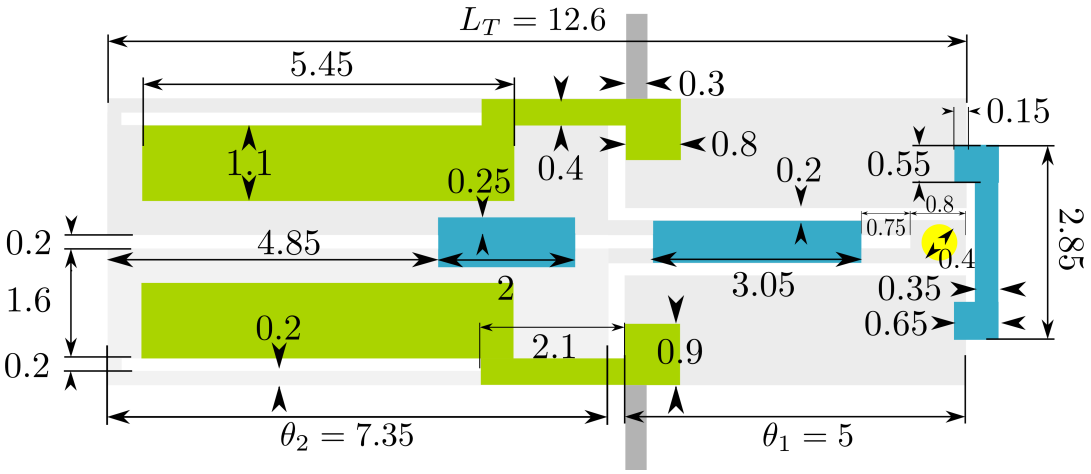


Figure 4.21: 1.2/2.4 GHz design. Inter-resonator coupling depending on the area of CP_1 and CP_2. (M) Magnetic dominant mode (see Fig. 4.22 for resonator's dimensions). $h_c = 0.025$ mm, $h = 0.2$ mm, $\epsilon_r = 3$.

mm^2, respectively, with $h_c = 0.025$ mm. As previously discussed, the inclusion of this two patches modifies the resonant frequencies, as well as the use of a common ground via, so at this stage, the dimensions of the resonator have to be adjusted to compensate this effect and match the desired center frequencies, 1.2 and 2.4 GHz in this case. The final value for L_T is set to 12.6 mm and R_θ, to 1.47 (ignoring the length reduction in line section A to include the grounding via patch).

Regarding k, from (4.2) the values $k_1 = 0.136$ and $k_2 = 0.109$ are calculated. As in the previous step, the dimensions of CP_1 and CP_2 can be obtained from Fig. 4.21, being the point where both curves cut each other, i.e. $CP_1 = 0.6$ mm^2 and $CP_2 = 0.4$ mm^2.

Once the sizes for the resonators and patches are fixed, the stop-band can be expanded by moving the coupling patches along the symmetry plane. As the structure is so compact, additional coupling paths are generated, producing additional transmission zeros. However, the values for the coupling patches would require further tuning. The completed design and dimensions are shown in Figure 4.22. Furthermore, the physical realization for C_{TZ} (see Sections 4.4 and 4.5) for splitting the inter-band TZ is also shown.



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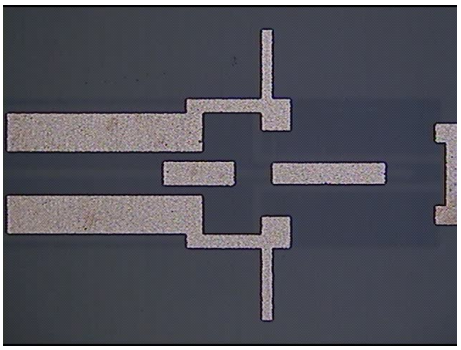

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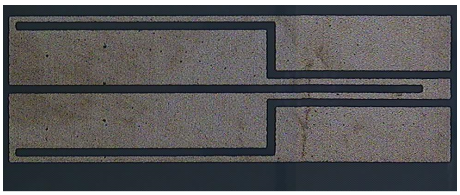
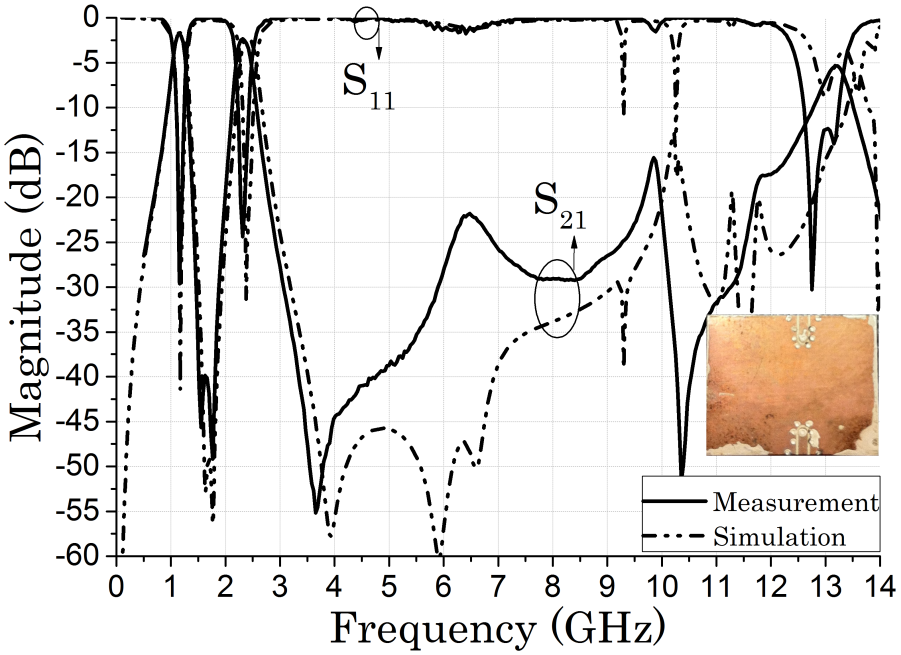
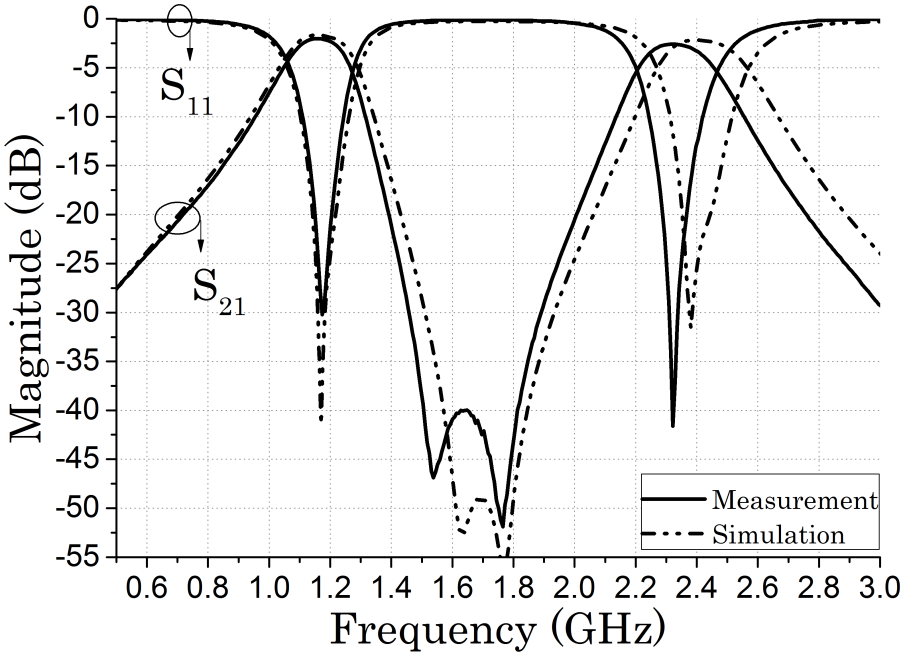


(c)

Figure 4.22: 1.2/2.4 GHz design details (a) Dimensions summary (in mm) (b) Top-view picture of the etched middle layer (c) Etched resonator (bottom-view of the middle layer)



(a)



(b)

Figure 4.23: 1.2/2.4 GHz design. Simulation vs. measurements (a) Wideband response. Fabricated device (b) Passbands detail

4.8.2 Simulation and results

Results show good agreement between the simulated and measured results (Fig. 4.23). It is demonstrated how the in-band second-order TZ splits into two TZ, with a separation proportional to the capacitance C_{TZ}. A slight shift in the second band's center frequency can be appreciated, due to small over-compression of the 25 μm core-film layer.

4.9 Wi-Fi dual band filter

In order to further demonstrate the capabilities of this filter topology, a new design is proposed, aiming at matching WiFi passbands:

- First passband centered in 2.4 GHz with a 8% fractional bandwidth.
- Second passband centered in 5 GHz with a 5% fractional bandwidth.
- Return loss 20 dB.
- Stop band after second passband up to, at least, 6 times the center frequency of the first passband.

4.9.1 Design

For this design, same considerations towards fabrication as in Section 4.8 are taken. Substrate thickness, layer distribution, and values for high- and low-impedance lines are kept the same.

Previously described design steps are followed (refer to Sections 4.7 and 4.8 for details). In this case the resonator, after optimization, is designed with $L_T = 6$ mm and $R_\theta = 1.57$.

Using the normalized parameters $g_0 = 1.0$, $g_1 = 0.665$, $J_1 = 0.905$, for a return loss of 20 dB, the required values for Q_{e1} and Q_{e2} are 8.3 and 13.3 from (4.1), corresponding to SP_1 and SP_2 calculated as 0.95 mm^2 and 0.3 mm^2 (Fig. 4.24). Regarding the coupling coefficient, required values of $k_1 = 0.109$ and $k_2 = 0.068$ correspond to $CP_1 = 0.15$ mm^2 and $CP_2 = 0.16$ mm^2 (Fig. 4.25). As discussed

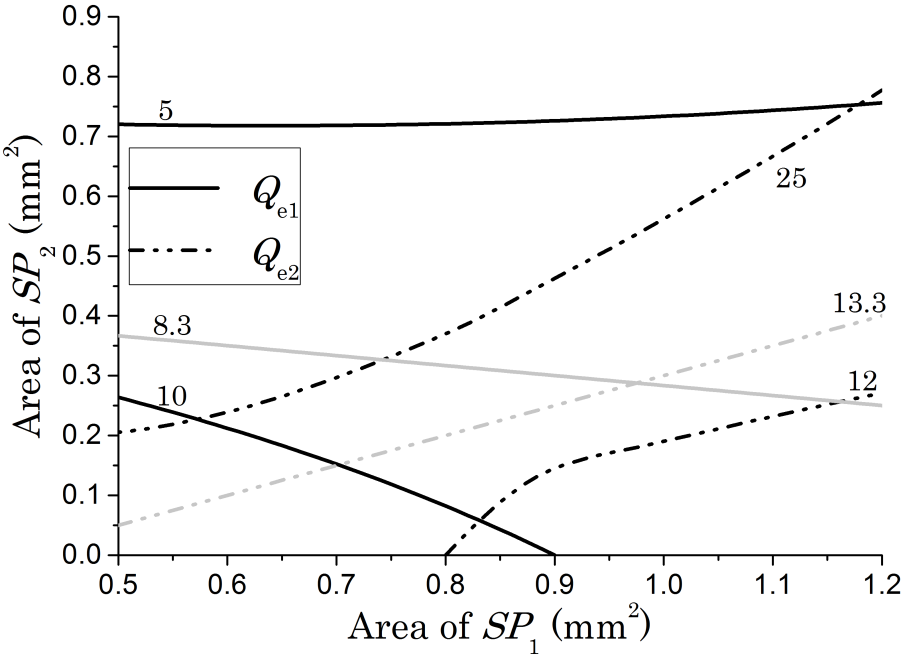


Figure 4.24: WiFi design. External quality factor (see Fig. 4.26 for resonator's dimensions). $h_c = 0.025$ mm, $h = 0.2$ mm, $\epsilon_r = 3$.

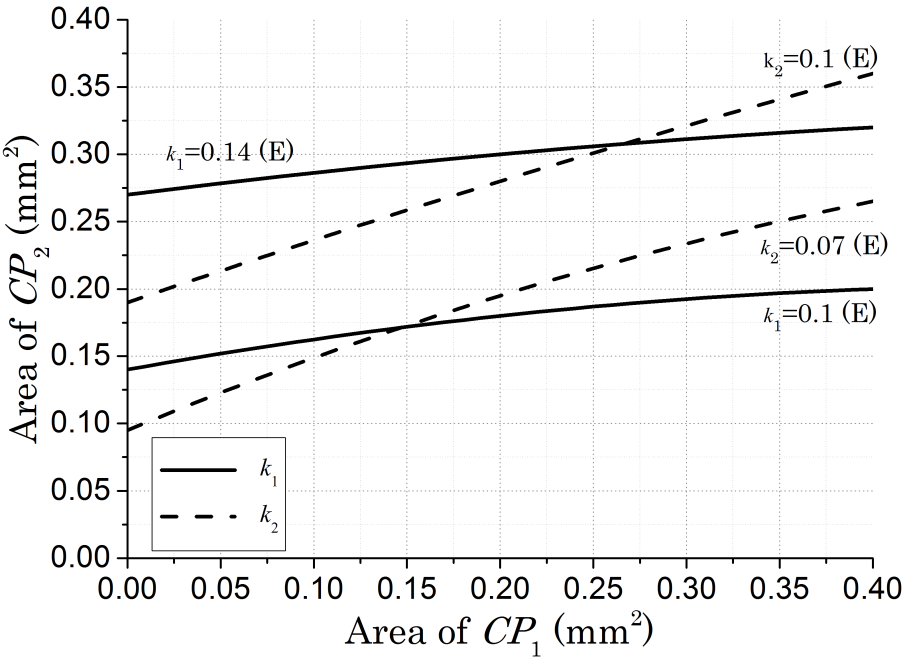
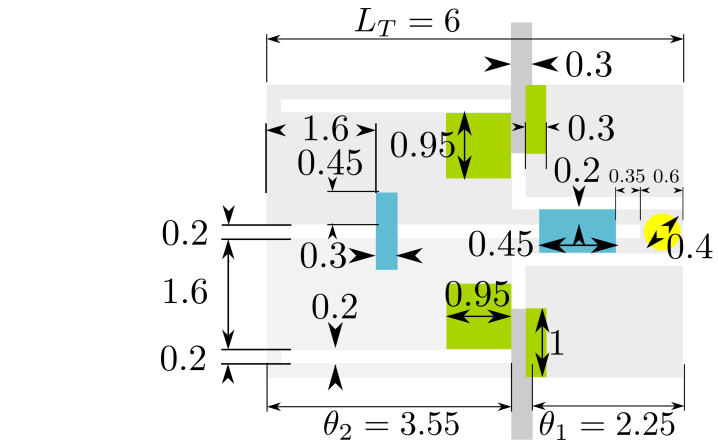


Figure 4.25: WiFi design. Inter-resonator coupling depending on the area of CP_1 and CP_2. (M) Magnetic dominant mode (see Fig. 4.26 for resonator's dimensions). $h_c = 0.025$ mm, $h = 0.2$ mm, $\epsilon_r = 3$.



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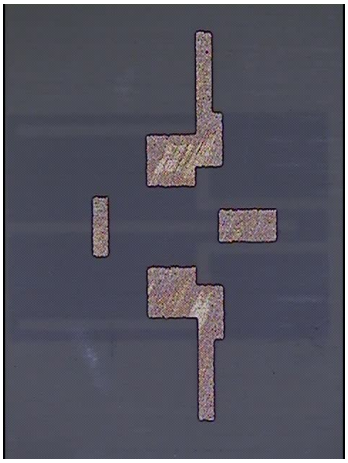

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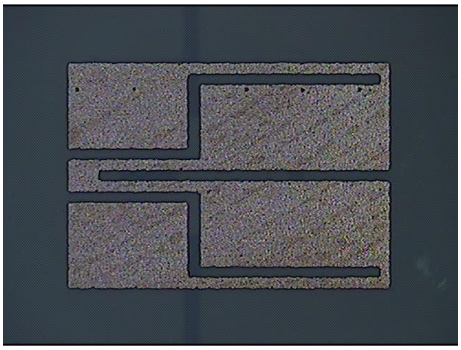


(c)

Figure 4.26: WiFi design details (a) Dimensions summary (in mm) (b) Top-view picture of the etched middle layer (c) Etched resonator (bottom-view of the middle layer)

for the previous design, further improvement can be obtained for the stopband by adjusting the position of the patches, and eventually, their sizes. Final dimensions for the design after optimization are shown in Figure 4.26.

4.9.2 Simulation and results

Results show excellent agreement between the simulated and measured results (Fig. 4.28). Only noticeable difference is in the return loss levels, possibly due to the manufacturing quality of the signal via transitions.

4.10 Fabrication

Both designs have been manufactured in a single experiment as they share the same layer-distribution settings (Fig. 4.27b), following the process from Chapter 2. Mask for the prototypes contains two samples of the former design, and three of the WiFi one (Fig. 4.27a). Mask for the CPW and ground layers are omitted (refer to Chapter 2).

Finished prototypes have a very low profile (0.4 mm) and a small footprint of 15.8×10.2 mm^2 the first design, and 7.5×11.2 mm^2 the second, both including packaging.

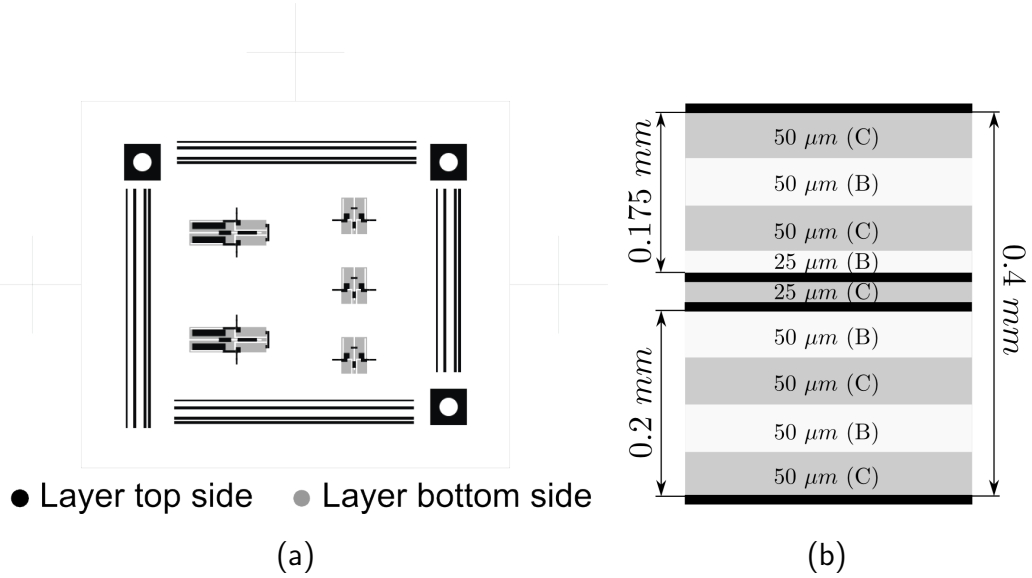
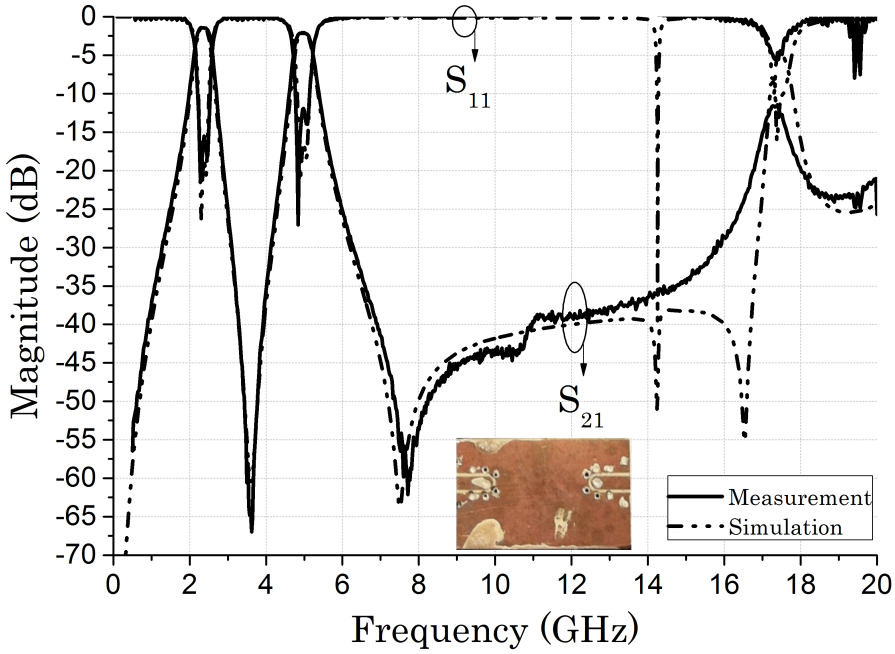
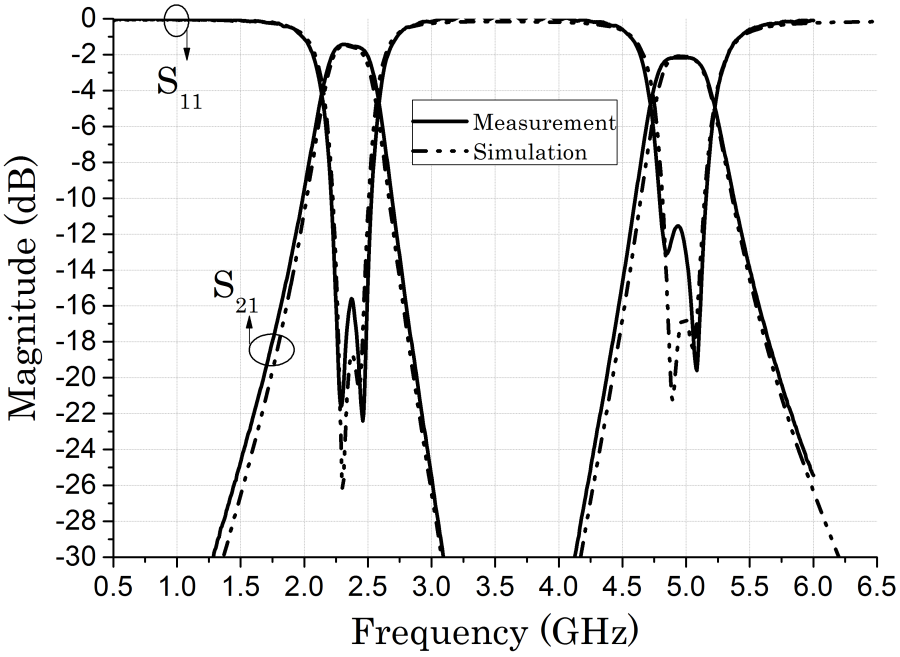


Figure 4.27: Mask and layer distribution for fabrication. (C=Core film, B=Bonding film)



(a)



(b)

Figure 4.28: WiFi design. Simulation vs. measurements. (a) Wideband response. Fabricated device (b) Passbands detail

4.11 Conclusions

In this chapter a novel compact structure for designing self-packaged dual-band filters has been presented. The design is based on a FMSIR used as a dual-mode resonator. Methods for obtaining the required inter-resonator couplings, and source coupling have also been discussed.

FMSIR working principle has been analysed, and demonstrated how it is capable of producing wider stopbands by shifting the second harmonic away from the fundamental and first resonant modes, which are used for producing the passbands. Furthermore, with appropriate tuning, it is capable of resonating at the same fundamental frequency as a conventional quarter-wavelength resonator, with a reduced footprint.

The approach of using metal patches above the resonator for producing required couplings is demonstrated. Moreover, the use of two different patches, allows for independent control of each band.

The previous concepts have been demonstrated with the design of two dual-band filters. Results obtained show high correlation with the simulations, showing deep out-of-band rejection and a wide stopband after the second passband. Comparison to other reported filters is summarized in Table 4.3, showing a big footprint saving by using this approach.

Table 4.3: Dual-band filters comparison

Ref.	Center freqs. (GHz)	FBW 1/2 (%)	IL (dB)	Size (λ_g^2)	Height (mm)	20 dB stop-band
[4]	2.45/5.5	8.1/21.8	1.5/1.2	0.02	0.76	N/A
[8]	1.2/3.5	Tunable	2.79/2.96	0.013	0.635	$9.84f_0$
[11]	2.45/5.2	11.4/11.3	2.2/1.1	0.0035	0.8	N/A
[12]	1.8/3.5	14/10	0.8/0.9	0.018	0.81	N/A
Section 4.8	1.2/2.4	10/8	1.79/2.37	0.0044	0.4	$8f_0$
Section 4.9	2.4/5	8/5	1.42/2.16	0.006	0.4	$7f_0$

FBW=Fractional bandwidth; IL=Insertion loss;

f_0=Lower center frequency; λ_g=Guided wavelength at f_0

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Chapter 5

Clean-up Low Pass Filter

5.1 Introduction

Low pass filters (LPF) are a key element in order to eliminate spurious resonances and unwanted passbands originated by intermodulation or the intrinsic nature of distributed resonators. Often they are chained to some other components within a system, so they are required not to introduce significant distortion or losses in the signal path.

Ideally, a LPF would let signals up to a certain cut-off frequency (f_c) pass through it transparently, rejecting any frequency higher than that f_c. However, in the real world, it is not the case and some trade-offs have to be met. Factors of merit in a LPF are low insertion loss (IL), sharp transition between passband and stopband, and the width and rejection level of the stopband. Depending on the requirements of a given application, the LPF design would prime some merits over the others.

A clean-up LPF is a type of LPF intended to be used in combination with some other filter or system. Its function is merely suppressing higher resonant modes without reducing the power of the initial signal. As such, low IL and a wide, deep rejection stopband is expected, but the requirements for the transition can be relaxed. Considering the previous, the aim of the work covered in this chapter is to design a compact, inexpensive, self-packaged LPF, focusing on the rejection levels of the stopband while maintaining a low IL.

One of the main concerns when designing a LPF is the suppression of higher harmonics and providing a wide stopband. Extensive research has been carried towards this

aim using different approaches. A popular approach is cascading successive LPFs with different cutoff frequencies [1–5]. A different method is employed in [6–10], where several transmission zeroes (TZs) are inserted in the stopband by including resonating elements, cancelling spurious harmonics. Furthermore, defected ground structures (DGS) are also investigated [11–13] to produce a wide stopband. However, the latter have the inconvenience of breaking the ground plane, and potentially increasing the radiation of the filter.

Even though the aforementioned LPFs provide a wide stopband, most of them are in the region of 20 dB for the rejection level, which would not meet the requirements for a more demanding clean-up filter. Work reported in [5, 13, 14] achieves deeper rejection levels, being the latter highly demanding in terms of fabrication technology.

Also key to a LPF is the selectivity, or how short in frequency is the transition from the passband to the stopband. Previously referenced work provide very sharp transitions [5–8,10,12,15], at the cost of lower performance on some other aspects like return loss (RL), rejection level, or stopband bandwidth. Despite being desirable, a sharp cutoff is not crucial in a clean-up filter.

For developing the filter, a structure based on the principle of destructive interference [1, 3, 16] is applied, composed of a pair of coupled lines and a feedback impedance. This kind of structure has been investigated as an impedance transformer [17] replacing the loop line for a two-section stepped impedance line. Additionally, a similar structure has been reported in [3], using different outputs from the coupled lines.

Along this chapter, the proposed, enhanced basic structure is described, progressively introducing modifications and discussing the improvements in performance until reaching the final proposed design. Lastly, two filters based on the discussion are designed, fabricated, and measured in order to validate the approach.

5.2 Theoretical background

Interference is a phenomenon in which two or more waves are superposed producing a combined result. The resulting wave could have larger amplitude than the original ones, i.e. constructive interference, or could result in cancellation, i.e. de-

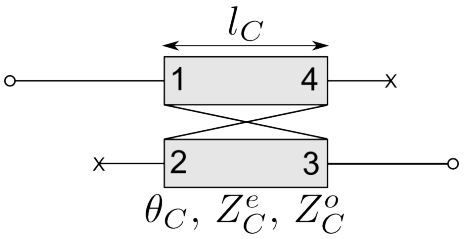


Figure 5.1: Coupled lines configuration

structive interference. In recent years, signal-interference techniques have become a suitable alternative to coupled-resonator arrangements to realize microwave filters with improved features [1]. In these circuits, the input signal is split into several components propagating through different signal paths, and then combined. Thus, filtering action is derived from the combination of the signal components.

5.2.1 Coupled lines

A pair of coupled lines with opposite ends used as source and load, and the remaining ends left open (Fig. 5.1), behaves as a band-pass with center bands when the electrical length is $\pi/2$ and $3\pi/2$, related to the wavelength equal to the physical length of the coupled lines. The amount of power transferred from source to load depends on the coupling coefficient (k), increasing as the coupling is tighter. At 0 and π no power is transmitted.

5.2.2 Filtering structure with generic loop-impedance

The structure used for producing the mentioned interference is composed of a pair of broadside coupled lines plus a generic two-port impedance connecting alternate ends of the coupled lines (Fig. 5.2). Thus, the input signal travels, at least, through two different paths: firstly through the pair of coupled lines, and secondly, through the loop formed with each of the coupled lines individually and the feedback impedance. The feedback impedance (Z') is fully defined by its Z-parameter matrix:

$$Z' = \begin{pmatrix} Z'_{11} & Z'_{12} \\ Z'_{21} & Z'_{22} \end{pmatrix} \tag{5.1}$$

Assuming the feedback impedance network is symmetrical and reciprocal, then $Z'_{11} = Z'_{22}$ and $Z'_{12} = Z'_{21}$. Also, if lossless, non-dispersive propagation is considered,

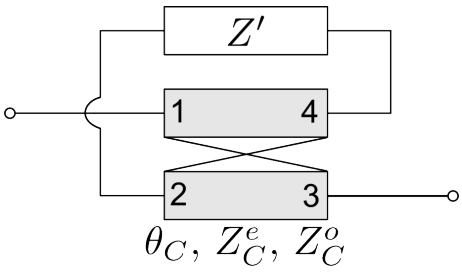


Figure 5.2: Feedback interference generic structure

the complete 2-port filtering structure can be defined in terms of its Z-parameters (Z) as follows:

$$Z = \begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} \tag{5.2}$$

Once defined the two components of the structure, and applying elementary circuit analysis and algebra (see Appendix A.1), impedance parameters for the generic structure are found as:

$$\begin{aligned} Z_{11} = Z_{22} &= -jZ_C \frac{\alpha_{11} + \beta_{11}}{\Delta} \\ \alpha_{11} &= q(Z'^2_{11} - Z'^2_{12} + Z_C^2)\sin\theta_C \cos\theta_C \\ \beta_{11} &= jZ_C Z'_{11}[(1+q^2)\sin^2\theta_C - q^2] \end{aligned} \tag{5.3}$$

$$\begin{aligned} Z_{12} = Z_{21} &= -jZ_C \frac{\alpha_{12} + \beta_{12}}{\Delta} \\ \alpha_{12} &= qk(Z'^2_{11} - Z'^2_{12} - Z_C^2)\sin\theta_C \\ \beta_{12} &= jZ_C Z'_{12}(k^2\sin^2\theta_C - q^2) \end{aligned} \tag{5.4}$$

$$\begin{aligned} \Delta = &[(Z'^2_{11} - Z'^2_{12})q^2 + Z_C^2]\sin^2\theta_C - Z_C^2 q^2 \\ &+ j2qZ_C(Z'_{12}k - Z'_{11}\cos\theta_C)\sin\theta_C \end{aligned}$$

where θ_C is the electrical length of the coupled lines, and $q = \sqrt{1-k^2}$. Note that the structure is reciprocal, provided the feedback impedance is reciprocal itself. For

convenience, let λ_r the reference wavelength, defined as the wavelength that equals the physical length of the coupled lines:

$$\lambda_r = l_C \tag{5.5}$$

Electrical lengths in the structure will be defined based on this value. Assuming TEM mode, propagation constant (β) is defined as [18]:

$$\beta = \frac{2\pi}{\lambda} \tag{5.6}$$

Since, by definition, $\theta = \beta l$, (5.5) and (5.6) may be conveniently combined as:

$$\theta_C = \frac{2\pi}{\lambda_r} l_C \tag{5.7}$$

It is known that guided wavelength can be approximated by [18]:

$$\lambda = \frac{300}{f(GHz)\sqrt{\epsilon_{re}}} mm \tag{5.8}$$

Therefore, using (5.7) and (5.8), electrical length can be mapped to frequency as:

$$f(\theta)(\text{GHz}) = \frac{300}{l_C(\text{mm})\sqrt{\epsilon_{re}}} \frac{\theta(\text{rad})}{2\pi} \tag{5.9}$$

where ϵ_{re} corresponds to the effective dielectric constant of the substrate.

Scattering parameters (S-Parameters) can be obtained from the Z-parameters using the well known formulas:

$$S_{11} = S_{22} = \frac{Z_{11}^2 - Z_0^2 - Z_{21}^2}{(Z_{11} + Z_0)^2 - Z_{21}^2} \tag{5.10a}$$

$$S_{21} = S_{12} = \frac{2Z_{21}Z_0}{(Z_{11} + Z_0)^2 - Z_{21}^2} \tag{5.10b}$$

where Z_0 is the reference impedance. Note Z_{ij} are a function of θ_C, therefore S_{mn} are also a function of θ_C. This dependency is omitted in (5.10a) and (5.10b) for readability.

5.2.3 Transmission zeros

Transmission zeroes are the points in frequency where all the transmitted power is reflected back to the source. Source is virtually disconnected from the load. These singular frequencies have an impact on the rejection levels of the stopband depending on their distribution. From (5.10b) it is immediate to demonstrate there is no power transmission from source to load when $Z_{21} = 0$. Therefore, from (5.4), the condition for transmission zero is obtained as:

$$qk(Z'^2_{11} - Z'^2_{12} - Z_C^2)\sin\theta_C + jZ_C Z'_{12}(k^2\sin\theta_C - q^2) = 0 \tag{5.11}$$

5.2.4 Cutoff frequency

Cutoff frequency (f_C) is defined as the frequency where the magnitude of the transmitted power drops to half the input power, equivalent to 3 dB loss. In terms of (5.10b), f_C can be written as:

$$|S_{21}(f_C)|^2 = 0.5 \tag{5.12}$$

Therefore, at f_C, the following condition is true:

$$2Z_0|Z_{21}(f_C)| = 0.707|(Z_{11}(f_C) + Z_0)^2 - Z_{21}^2(f_C)| \tag{5.13}$$

5.3 Uniform loop-line

Building up on the previous discussion, this section covers the behaviour of the filtering structure when the feedback impedance is replaced by an uniform transmission line (Fig. 5.3), referred to as *loop-line*. A transmission line is a reciprocal structure defined in terms of Z-matrix as:

$$Z' = \begin{pmatrix} Z'_{11} & Z'_{12} \\ Z'_{21} & Z'_{22} \end{pmatrix} = \begin{pmatrix} -jZ_L\cot\theta_L & -jZ_L\csc\theta_L \\ -jZ_L\csc\theta_L & -jZ_L\cot\theta_L \end{pmatrix} \tag{5.14}$$

where Z_L is the characteristic impedance, and θ_L is the electrical length defined as:

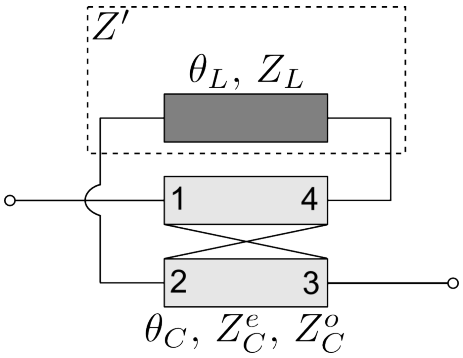


Figure 5.3: Filtering structure with uniform transmission line

$$\theta_L = \frac{2\pi}{\lambda_r} l \tag{5.15}$$

where l is the physical length of the loop-line.

5.3.1 Transmission zeros

Designing the stopband requires an analysis of the number and location of TZs. As such, by replacing (5.14) in (5.11), the condition for TZ is obtained:

$$\sin(\theta_L) = \frac{Z_L Z_C}{(Z_L^2 - Z_C^2)\frac{q}{k}} \frac{(\frac{q}{k})^2 - \sin^2\theta_C}{\sin\theta_C} \tag{5.16}$$

For convenience, R is defined as the length ratio between the loop-line and coupled lines:

$$R = \frac{\theta_L}{\theta_C} = \frac{l}{l_C} \tag{5.17}$$

Furthermore, the impedance ratio between the loop-line and the coupled lines is defined as:

$$R_Z = \frac{Z_L}{Z_C} \tag{5.18}$$

By replacing (5.17) and (5.18), (5.16) can be rewritten as:

$$\sin(R\theta_C) = \frac{R_Z}{(R_Z^2 - 1)\frac{q}{k}} \frac{(\frac{q}{k})^2 - \sin^2\theta_C}{\sin\theta_C} \tag{5.19}$$

From (5.19) it is easy to show the symmetry of the response for integer values of R around $\theta_C = \pi$. Moreover, if R is odd, the response will also be symmetric around $\theta_C = \pi/2$. Also interesting to note that the maximum number of TZs in the interval $(0, \pi)$ is $R + 1$.

If the value of R is fixed to 3, a compact structure with up to four TZs is obtained. From this point $R = 3$ is assumed, unless stated. The condition for TZs in such conditions can be obtained from (5.19) as follows:

$$4\sin^4\theta_C - (3 + Z_x\frac{k}{q})\sin^2\theta_C + Z_x\frac{q}{k} = 0 \tag{5.20}$$

$$Z_X = \frac{Z_L Z_C}{Z_L^2 - Z_C^2} = \frac{R_Z}{R_Z^2 - 1}$$

By solving (5.20) for θ_C, the location of the four TZs is found as:

$$\theta_{TZ} = \sin^{-1}\left(\pm\sqrt{\frac{3 + Z_X\frac{k}{q} \pm \sqrt{(3 + Z_X\frac{k}{q})^2 - 16Z_X\frac{q}{k}}}{8}}\right) \tag{5.21}$$

The position of the TZs are determined by k and R_Z, and depending on their values, they could be real or imaginary. Attending to this, and considering the number of TZ's within the $0 < \theta_C < \pi$ range, three different working regions are identified by finding the limits in (5.21) between real and imaginary solutions (Fig. 5.4):

- 4-TZ region, when

$$k < \frac{R_Z}{\sqrt{R_Z^2 + 1}}$$

$$(3 + Z_X\frac{k}{q})^2 > 16Z_X\frac{q}{k} \tag{5.22}$$

$$R_Z > \frac{\sqrt{5}}{2}$$

- 2-TZ region, when

$$k > \frac{R_Z}{\sqrt{R_Z^2 + 1}} \tag{5.23}$$

- No real TZs, if the previous conditions are not met.

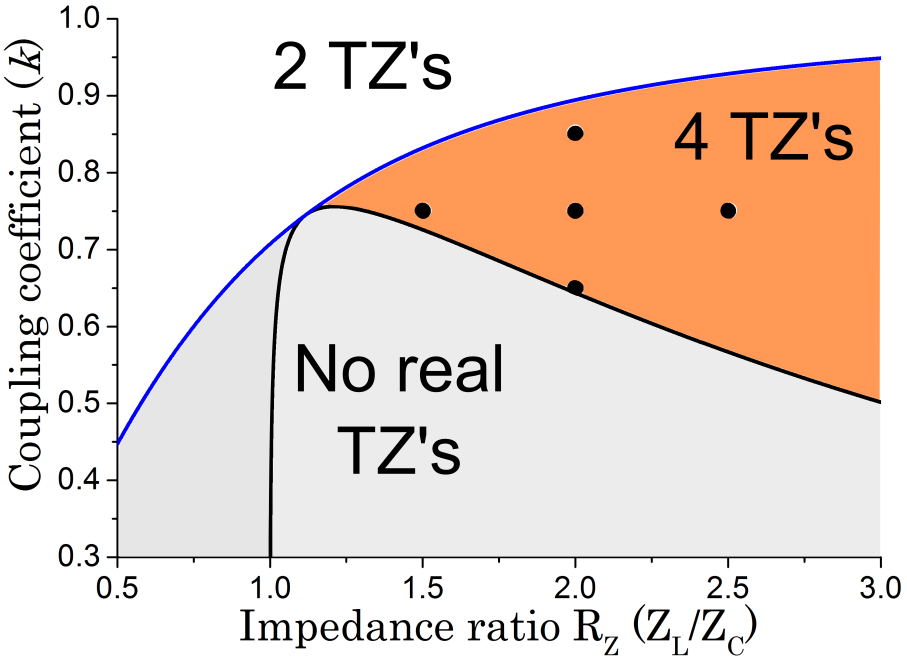


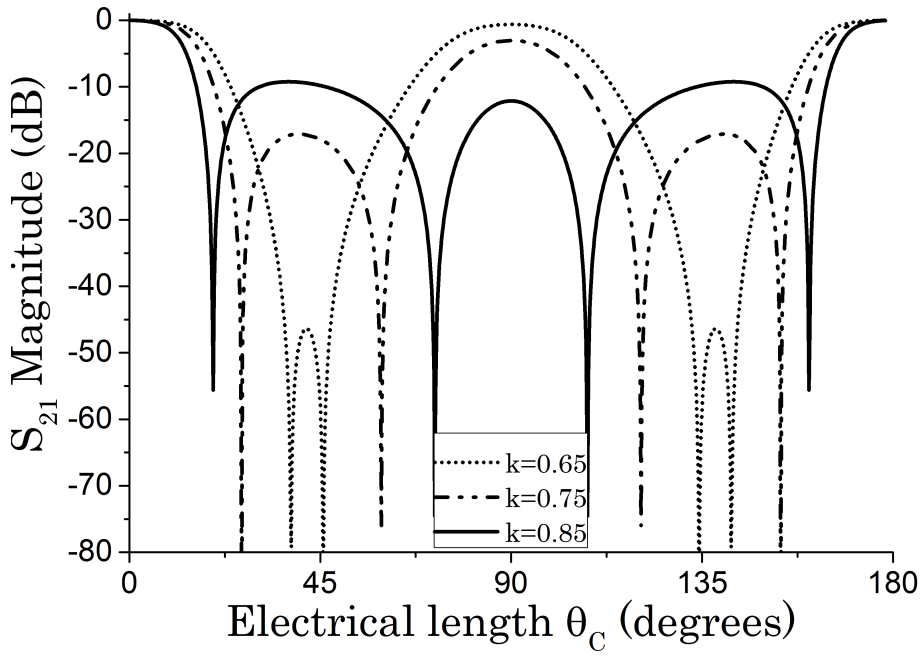
Figure 5.4: Different regions depending on the number of TZs. (•) in the 4-TZs region correspond to plots in Fig. 5.5.

Note how the location of TZs is independent from Z_C. However, variations in this parameter would affect the rejection levels. It is observed in theoretical model simulations that lower values of Z_C would increase the rejection between the first and last pair of TZs, while reducing it between the second and third TZ.

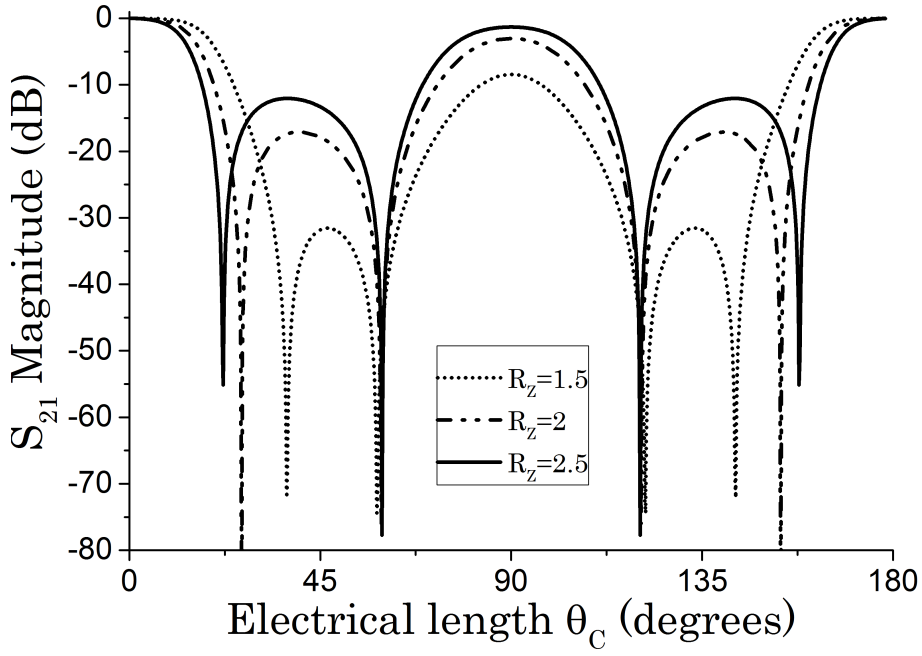
In order to obtain a wide and deep rejection band, the 4 TZs region is the most interesting one. Several pairs of R_Z and k within it are plotted in Fig. 5.5 (also marked on Fig. 5.4). It can be appreciated how variations of k would equally affect all the TZs, while variations of R_Z would mainly affect the first and fourth TZ, having a negligible effect on the inner pair of TZs. As a rule of thumb, higher values of k increase the stopband width and selectivity, reducing the rejection level.

Matched-impedance case

As discussed, location of TZs depends on three parameters, namely R, R_Z, and k. However, from (5.16) an interesting property is derived: if $Z_L = Z_C$, i.e. matching the loop-line impedance to the coupled-lines characteristic impedance, two TZs are generated in $\theta_C(0, \pi)$ regardless the value of R, and their positions depend exclusively on k (Fig. 5.6), as demonstrated in:



(a)



(b)

Figure 5.5: TZ variations (a) for different values of k (Z_C=30 Ω, $R_Z = 2$) (b) for different values of R_Z ($k = 0.75, Z_C = 30\ \Omega$)

$$Z_L = Z_C \implies R_Z = 1 \implies \theta_{TZ} = \arcsin\frac{q}{k} = \arcsin\frac{\sqrt{1-k^2}}{k} \tag{5.24}$$

Furthermore, as there is no dependency from R, the length of the loop-line has no effect on the location of the TZs. This pair of TZs are real for $k \geq 1/\sqrt{2}$ and symmetrically placed around $\theta_C = \pi/2$. The high value of k required to fulfil this condition makes this structure more suitable for broadside coupled lines using multilayer techniques, where higher coupling coefficients can be obtained. Since the position of the TZs is not affected by the length of the loop-line, this structure has possible applications as a phase-shifter.

5.3.2 Transmission maximum

In a lowpass filter design, the passband is equally as important as the stopband. In order to determine the location and number of the transmission maximums, it can be found from (5.10a), the transmission maximum (TM) condition is:

$$Z_{11}^2 - Z_{21}^2 = Z_0^2 \tag{5.25}$$

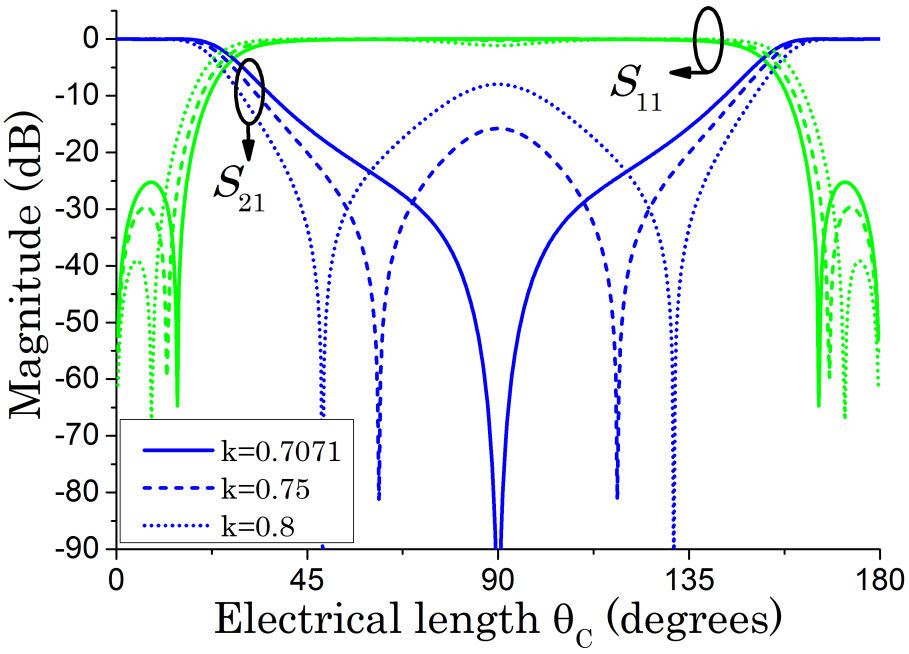
This expression can be rewritten as:

$$\frac{Z_0^2}{Z_C^2} = \frac{(\alpha_{11}+\beta_{11})^2 - (\alpha_{12}+\beta_{12})^2}{\Delta} \tag{5.26}$$

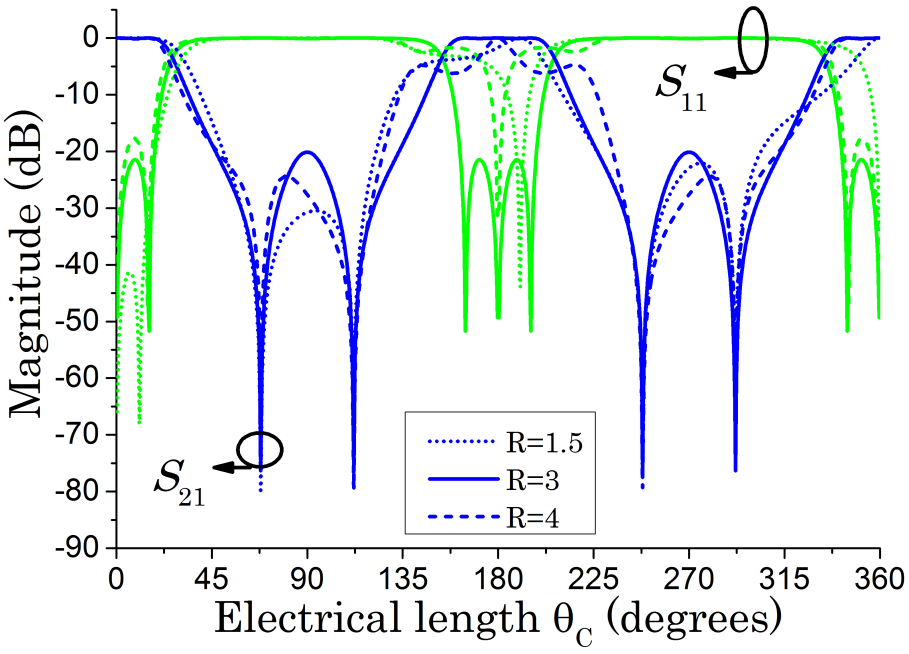
The right hand side of the expression only depends on θ_C and R_Z (assuming R_Z independent from Z_C), so the TM condition is dominated by Z_C. By using algebraic transformations, it can be demonstrated that for values of θ_C in the passbands, a maximum of two poles can be obtained, with one of them located at $\theta_C = 0$. Reducing Z_C will approximate the second TP to the cutoff frequency. Taking the limit when $Z_C = 0$, TM's are located at the roots of Δ. On the other end, taking the limit when $Z_C = \infty$, makes the two TP to meet at $Z_C = 0$.

5.3.3 Equal-ripple stopband

Having equal-ripple in the stopband is a desirable property in a LPF, as the level of undesired harmonics will be the same across the stopband, avoiding the need for



(a)



(b)

Figure 5.6: Filtering response with matched impedances ($Z_0 = 50\ \Omega$) (a) Variations of coupling coefficient ($R = 3$, $Z_L = Z_C = 30\ \Omega$) (b) Variations of length ratio ($Z_L = Z_C = 27.82\ \Omega$, $k = 0.733$)

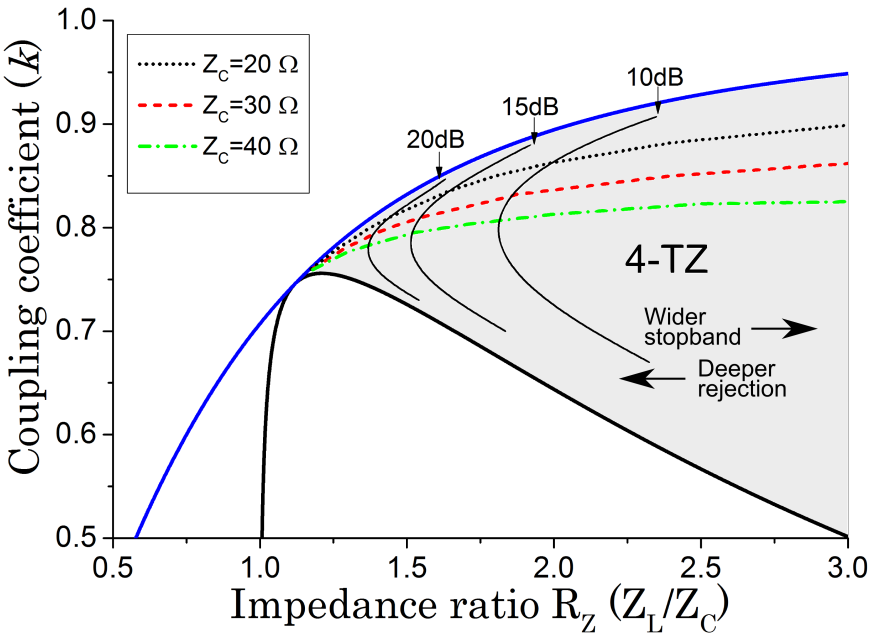


Figure 5.7: Equal-ripple design curves for uniform loop-line. dB label indicates level of equal-ripple rejection

using an equalizer in the host application. However, there is a trade-off between the width and the rejection level of the stopband. Wider stopband implies lower rejection levels and vice versa. Main design parameters of the filter are k and R_Z. However, k and Z_C are not independent, and high values of k usually are obtained for low values of Z_C. This fact reduces the flexibility in the design.

In order to analytically establish a condition that provides an equal-ripple in the stopband, S_{21} response is considered. It has been established that $R = 3$ and, therefore, S_{21} is symmetrical around $\theta_C = \frac{\pi}{2}$. At this frequency there is a local maximum between the second and third TZs. Thus, a possible approach for finding the equal-ripple condition is matching $S_{21}(\pi/2)$ with the value of S_{21} at the local maximum between the first two TZs (θ_M), which is equivalent to the local maximum between the third and fourth TZs due to the symmetry. However, mathematical derivation for this procedure leads to complicated and impractical expressions. Instead, design curves are derived based on interpolation (Fig. 5.7). In this figure, dashed lines represent the equal-ripple curves for a given value of Z_C, while the curves labelled in dB represent the equal-ripple rejection for combinations of k and R_Z. Note how for every pair (k,Z_C) there is only one value of R_Z that fulfils the equal-ripple condition.

5.3.4 Cutoff frequency

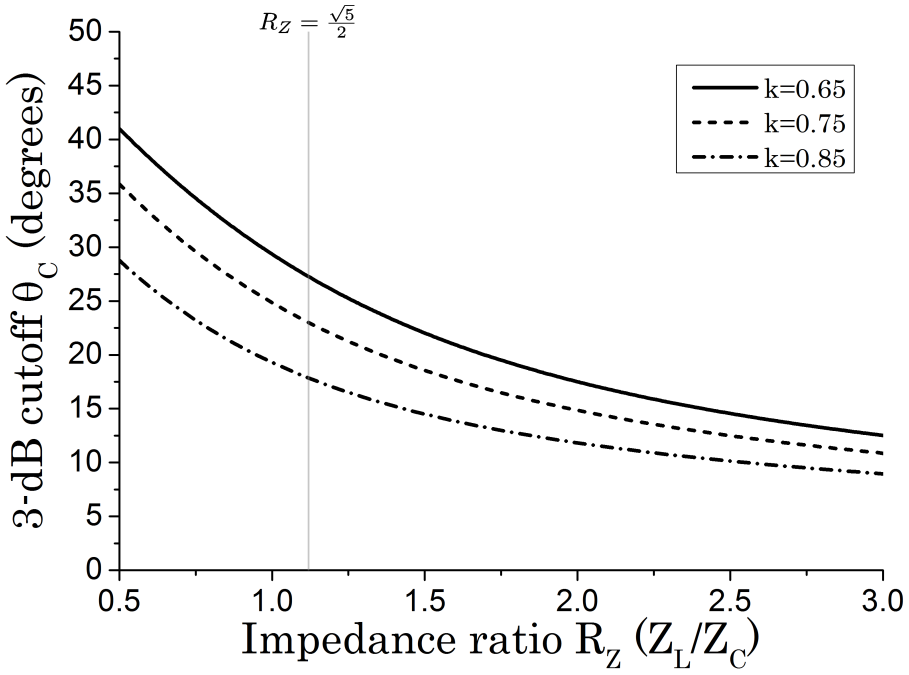
As R is fixed to 3, the response of the filter is symmetric around $\theta_C = \pi/2$. With this, we can determine the stopband BW depending on f_C as:

$$FBW = \frac{\pi - 2\theta_{3dB}}{\pi/2} \tag{5.27}$$

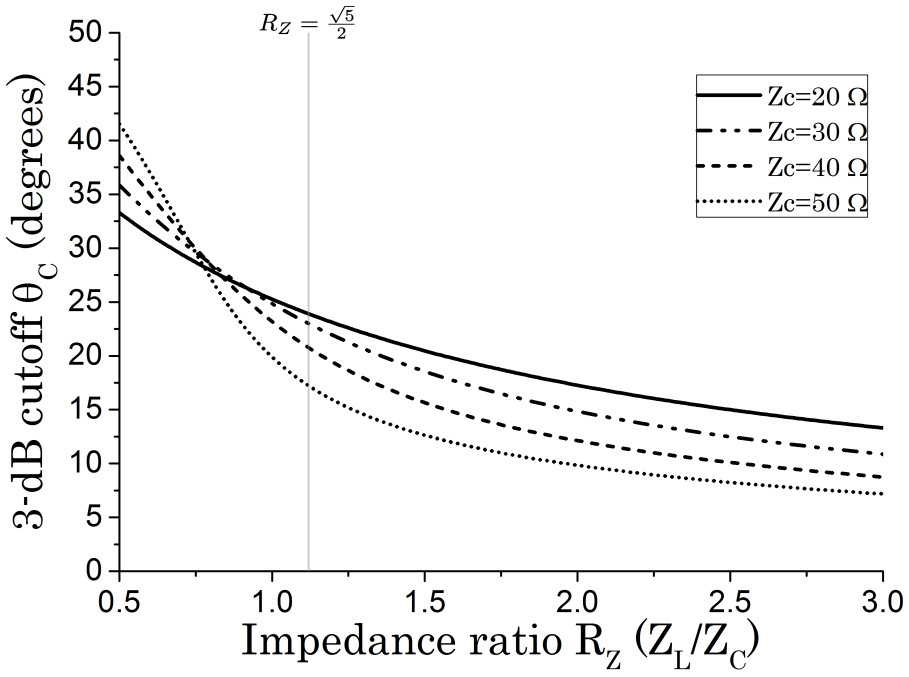
Or, as a function of cutoff freqency, as:

$$BW(f_C) = (\frac{\pi}{\theta_{3dB}} - 1)f_C \tag{5.28}$$

In order to determine the 3dB cutoff frequency, k, Z_C and R_Z are the key parameters. Fig. 5.8 shows different design curves for these parameters. According to the figures, both k and Z_C have similar effects on the cutoff frequency when working on the 4-TZs region, i.e. $R_Z > \sqrt{5}/2$, decreasing as R_Z increases. Moreover, they both can be combined to obtain the desired cutoff.



(a)



(b)

Figure 5.8: 3-dB cutoff frequency (a) for different values of k ($Z_C = 30\ \Omega$) (b) for different values of Z_C ($k = 0.75$)

5.4 Stepped-impedance loop-line

Likewise the previous section, the uniform loop-line is now replaced by a three-section impedance line (Fig. 5.9). For simplicity, the length of the middle section is equal to the length of the coupled lines ($\theta_2 = \theta_C$). The other two sections have the same length (θ_1). Furthermore, we can define the impedance ratio of the loop line as:

$$R_S = \frac{Z_2}{Z_1} \tag{5.29}$$

where Z_2 is the impedance of the line section parallel to the coupled lines, and Z_1 the impedance of the remaining two sections. Following the convention for the uniform-line case, R_Z is defined now as Z_1/Z_C. In this way, the response from the coupled-line loop unit can be initially determined by the coupled lines parameters (θ_C, Z_C, k) and the loop line parameters (θ_1, R_Z, R_S).

The modification is particularly interesting when the length ratio (R) is fixed to 3, i.e. fixing $\theta_1 = \theta_2 = \theta_C$, as will be discussed in this section. Under this conditions, the Z-parameters for the loop line are:

$$\begin{aligned} Z'_{11} = Z'_{22} &= -jZ_1 \cot\theta_C \frac{(R_S+1)^2 \sin^2\theta_C - R_S}{(R_S+1)^2 \sin^2\theta_C - 2R_S - 1} \\ Z'_{12} = Z'_{21} &= jZ_1 \csc\theta_C \frac{R_S}{(R_S+1)^2 \sin^2\theta_C - 2R_S - 1} \end{aligned} \tag{5.30}$$

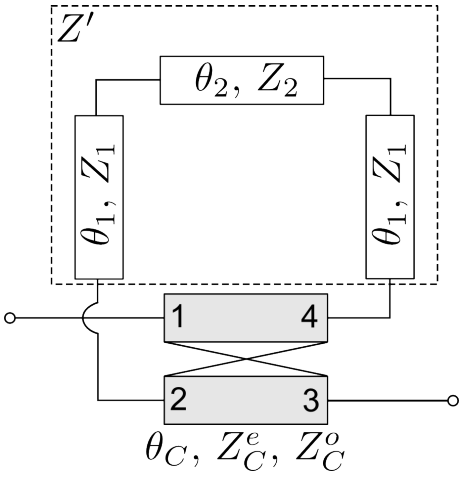


Figure 5.9: Filtering structure with stepped-impedance transmission line

5.4.1 Transmission zeros

As previously discussed, the structure is capable of producing up to four TZ's in the stopband and the response will be symmetric. The advantage introduced by this configuration is a better control over the response in the stopband as the position of the two inner TZ's can be adjusted with R_S without having too much impact on the outer ones, thus enabling the possibility of obtaining an equal-ripple stopband (Fig. 5.11).

As such, from (5.11) and (5.30) the condition for TZs is calculated as:

$$\frac{(R_S+1)^2}{R_S}\sin^4\theta_C - (Z_X\frac{k}{q} + 2 + \frac{Z_X}{Z_Y})\sin^2\theta_C + Z_X\frac{q}{k} = 0 \tag{5.31}$$

$$Z_X = \frac{Z_1 Z_C}{Z_1^2 - Z_C^2} = \frac{R_Z}{R_Z^2 - 1}$$

$$Z_Y = \frac{Z_2 Z_C}{Z_2^2 - Z_C^2} = \frac{R_Z R_S}{R_Z^2 R_S^2 - 1}$$

Note if $R_S = 1$, then $Z_X = Z_Y$ and this expression is equivalent to (5.20), as expected, since $R_S = 1$ corresponds to the uniform-line case. From (5.31), three different working regions, depending on the number of real TZs, can be identified:

- 4-TZ region, when

$$k < \frac{R_Z}{\sqrt{R_Z^2 + R_S^2}}$$

$$(\frac{Z_X}{Z_Y} + 2 + Z_X\frac{k}{q})^2 > 4\frac{(R_S+1)^2}{R_S}Z_X\frac{q}{k} \tag{5.32}$$

$$R_Z > \sqrt{\frac{R_S^2}{(R_S^2+1)^2} + 1}$$

- 2-TZ region, when

$$k > \frac{R_Z}{\sqrt{R_Z^2 + R_S^2}} \tag{5.33}$$

- No real TZs, if the previous conditions are not met.

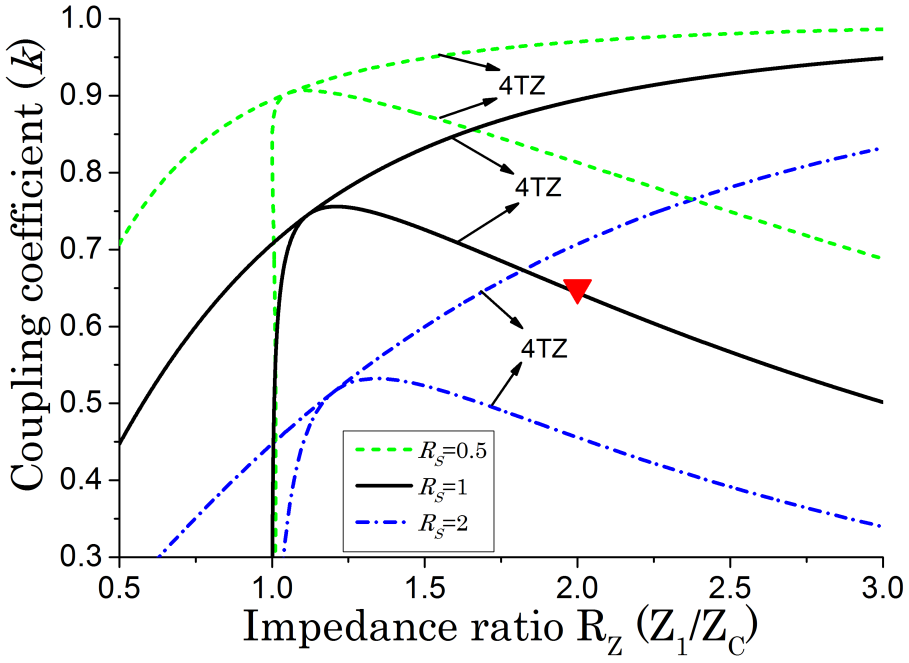


Figure 5.10: TZ regions for different values of R_S

As in the previous section, the different working regions are plotted in Fig. 5.10. It can be observed how they are similar to the uniform-line case, but the position is shifted over k. This effect suggests that similar responses can be obtained with lower k when this is compensated with higher values of R_S. Moreover, variations of R_S for fixed values of k, Z_C, and R_Z are depicted in Fig. 5.11. Further variations of k and R_Z have a similar effect as in the uniform line case. As an example, design values for the fabricated filters are marked. Note how the effect of R_S makes the design in Section 5.8 to have 4-TZ's, instead of the expected two in the uniform-line case.

5.4.2 Transmission maximum

Using a similar derivation as in the previous section, the right hand side of (5.26) in the case of a stepped-impedance line, depends on θ_C, R_Z, and R_S. The position of the second TM may be controlled by Z_C/Z_0 ratio, ranging from $Z_C = 0$ to the first root of Δ.

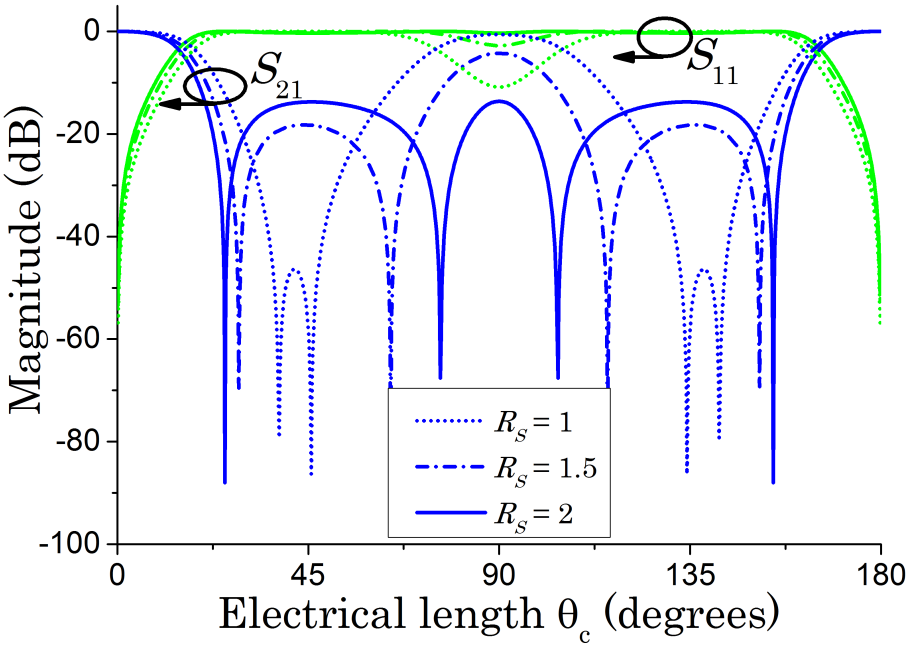


Figure 5.11: S-Parameters for different values of R_S ($k = 0.65, Z_C = 30\ \Omega, R_Z = 2$)

5.4.3 Equal-ripple stopband

Following the discussion for the case with an uniform loop-line, and provided the complexity of the expressions derived mathematically, a new set of design curves is obtained for the stepped-impedance loop-line (Fig. 5.12).

It has been demonstrated how the 4-TZ region is affected by R_S. This fact introduces a key advantage over the uniform loop-line case since the parameter choice for an equal-ripple response now includes a new degree of freedom.

5.4.4 Cutoff frequency

In the case of an uniform-line, the cutoff frequency (f_C) could be determined based on the (k, Z_C, R_Z) set of parameters. For a stepped-impedance line, R_S also has to be included in this group. Variations of this parameter have a similar effect to variations of k.

From (5.3) and (5.4) it can be found that the most relevant term is $Z_{11}'^2 - Z_{12}'^2$. In order to establish a relationship between the cutoff frequencies in the uniform- and the stepped-line cases the mentioned term may be matched at cutoff frequency, obtaining the following relationship:

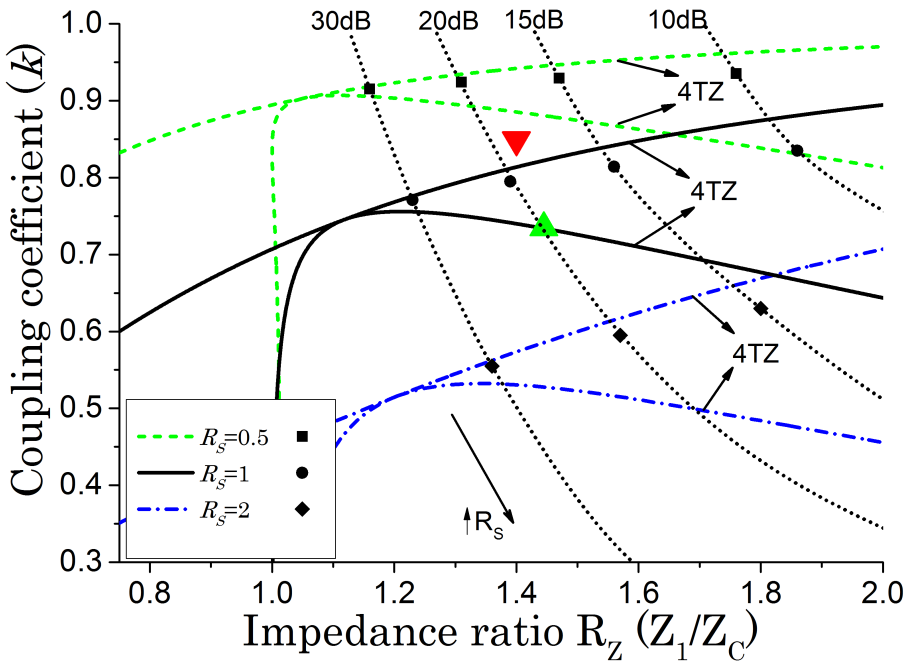


Figure 5.12: Equal-ripple design curves and TZ regions for different values of R_S. Dotted lines correspond to equal-ripple stopband with the labelled rejection for $Z_C = 28\ \Omega$. ($\bigtriangledown$) Section 5.8 design ($R_S = 0.83, Z_C = 20.97\ \Omega$) ($\bigtriangleup$) Section 5.9 design ($R_S = 1.26, Z_C = 28.14\ \Omega$)

$$\frac{R_{Zunif}^2}{R_{Zstep}^2} = \frac{(R_S+1)^2\sin^2\theta_0 - 2R_S - R_S^2}{(R_S+1)^2\sin^2\theta_0 - 2R_S - 1} \tag{5.34}$$

where θ_0 is the electrical length of the coupled lines (θ_C), at the matched cutoff frequency, R_{Zunif} and R_{Zstep} are the R_Z for the uniform- and stepped-line cases, and R_S is the impedance ratio of the stepped-line (see Appendix A.2).

Since we are matching both cases for the pass-band, θ_P would be a small value. Therefore, (5.34) can be simplified to:

$$\frac{R_{Zunif}^2}{R_{Zstep}^2} = \frac{2R_S + R_S^2}{2R_S + 1} \tag{5.35}$$

By establishing this relationship, the return loss for the stepped-line can match that of the uniform-line for a given pair (R_Z, R_S). As such, Fig. 5.8 can be used for estimating the cutoff frequency.

5.5 Design method

The design is carried in four steps:

- Determine required cutoff frequency in terms of θ_C, i.e. θ_{3dB}, that fulfills the requirements for FBW, and find l_C from (5.9).
- Design coupled lines (k, Z_C) and R_Z for the uniform-line case, i.e. R_{Zunif}, that provides the required θ_{3dB}, with the help of Fig. 5.8.
- Using Fig. 5.12 as a reference, estimate a new R_Z, i.e. R_{Zstep}, that meet the requirements for stopband rejection for the chosen k.
- Calculate R_S from (5.34) for the previously found R_{Zunif} and R_{Zstep}.
- Check the design parameters meet the conditions to work in the 4-TZs region and fulfill the requirements for bandwidth and rejection. If any of these restrictions is not met, the coupled lines must be re-designed.

5.6 Footprint reduction

The filtering structure is intended to be physically realised by sections of straight, uniform lines. However, footprint occupied with such a layout is not optimal. In this section two alternatives are covered in order to reduce the footprint.

Initially, the coupled lines are fed from the side edges. However, if the tapping points of the feeding lines are shifted towards the centre of the coupled lines, equivalent responses can be obtained with a reduced length of the loop line. Once the feed lines are shifted, the coupled lines can be considered divided into three sections (Fig. 5.13). In this case, the length ratio is related to the section between the feed lines (θ_{C2}). However, the loop-line is not divided into three uniform sections as section from the coupled lines between the input and the loop-line, is now included. This modification invalidates the discussion from previous sections and forces appropriate values for R_Z, R_S, and θ_{C1} to be found through optimization.

Furthermore, in order to achieve the same f_C after reducing θ_1, the length of the coupled-lines section (θ_C) will have to be increased. However, the reduction of θ_1 would be more significant, obtaining an overall size reduction when combined.

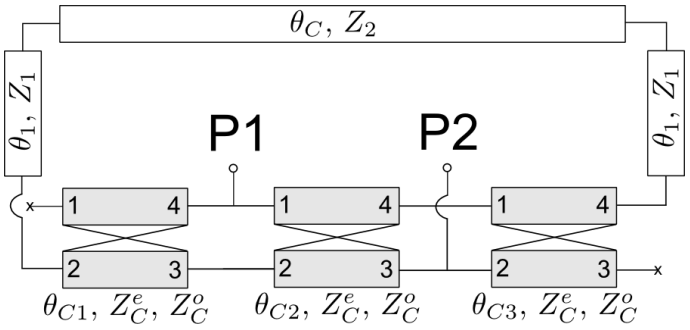


Figure 5.13: Footprint reduced loop-line structure ($\theta_C = \theta_{C1} + \theta_{C2} + \theta_{C3}$). P1 and P2 represent the I/O ports

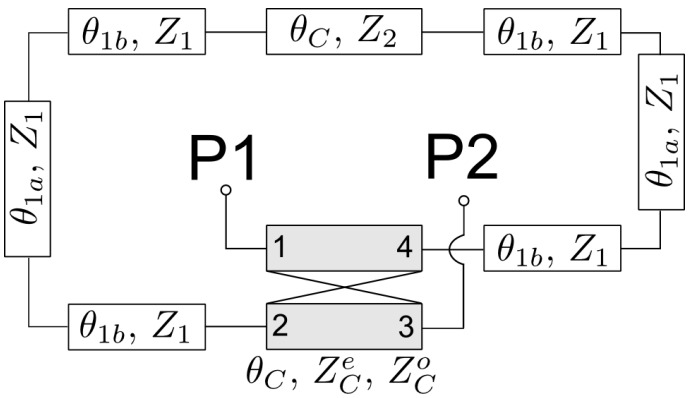


Figure 5.14: Footprint reduced loop-line structure, alternative layout ($\theta_1 = \theta_{1a} + 2\theta_{1b}$). P1 and P2 represent the I/O ports

With this method, the ends of the coupled lines are left open and each line behaves as a half-wavelength resonator. Thus, placing a limitation since excessive increase of θ_{C1} and θ_{C3} would make the resonant mode to appear in the stopband. This footprint reduction method is demonstrated with an example in Section 5.9.

Alternatively, the layout of the lines with θ_1 length can be modified and divided into three sections (Fig. 5.14), while keeping the original length ($\theta_1 = \theta_{1a} + 2\theta_{1b}$). By reducing the middle section, and dimensioning the rest accordingly, overall footprint reduction is obtained. As an example, making the middle section half its original size, and the other two sections equal to 1/4, dimension across coupled lines is increased by 50%, but dimension on the other axis is reduced by 50%, yielding a reduction of 25%.

5.7 Cascading

Even though the stopband achieved with a single unit can be in the region of 20-30 dB for a reasonable BW, this is not enough for many practical applications. One way of increasing the level of rejection without affecting the BW would be cascading two filters with identical characteristics. In this case, the order of the resulting filter is doubled, and so is the level of rejection, while keeping the BW intact.

When cascading two filters together with a section of transmission line, some resonances may appear. These resonances correspond to the frequencies where the input impedance (Z_{in}), looking into the filter from the interconnection point (Fig. 5.15) is matched ($Z_{in} = 0$), and the loop-structure self-resonating frequency, located at $\theta_C = \pi/2$ when $R = 3$.

The proposed idea for avoiding these resonances is matching them with the TZs. In

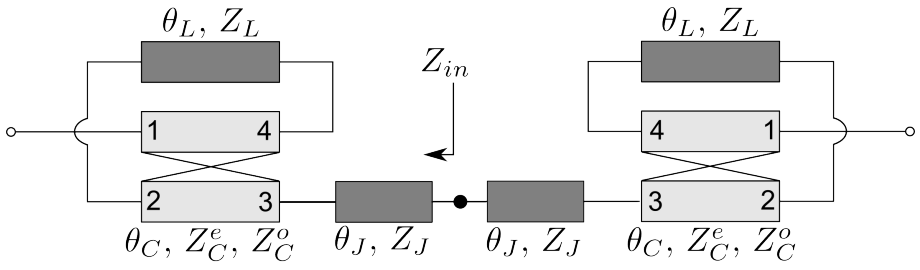


Figure 5.15: Cascaded model (uniform line case)

other words, making $Z_{in} = 0$ at the frequencies with TZ (θ_{TZ}). Z_{in}, when terminated in an arbitrary load (Z_{load}), is defined in terms of Z-parameters as:

$$Z_{in} = Z_{11} - \frac{Z_{12}Z_{21}}{Z_{11} - Z_{load}} \tag{5.36}$$

From (5.11), $Z_{21} = 0$ at TZ, so it is immediate to demonstrate:

$$Z_{in}(\theta_{TZ}) = Z_{11}(\theta_{TZ}) = Z_{22}(\theta_{TZ}) \tag{5.37}$$

assuming $Z_{21} = Z_{12}$.

The simplest form of matching network for this purpose is a uniform transmission line of a determined length (θ_J) and characteristic impedance (Z_J). Designing these parameters accordingly, at least the first TZ can be matched by using (5.38). The rest of possible resonances have to be matched by optimizing the structure. A demonstrating example is covered in Section 5.9.

$$\theta_J = \frac{\pi/2}{\theta_{TZ1}} \arctan \frac{Z_{in}(\theta_{TZ1})}{Z_J} \tag{5.38}$$

5.8 Interference-based LPF with 2 GHz cutoff frequency

In order to demonstrate the theory previously discussed, a design example will be introduced in this section. Requirements for this filter are:

- Cutoff frequency: 2GHz
- Stopband up to $9f_C$, equivalent to 160% fractional bandwidth (FBW)
- Equal ripple with 20dB rejection

5.8.1 Parameters design

Following the design method previously described, at the first step, and from (5.27), $\theta_{3dB} = 18^o$ for a 160% FBW is found. With this value, l_C that maps θ_{3dB} to 2GHz,

from (5.9), is 4.33 mm. Each of the three sections of the stepped-impedance loop-line have the same length as the coupled lines ($\theta_1 = \theta_2 = \theta_C$).

In the second step, coupled-lines parameters have to be designed, as well as the corresponding R_Z. In this case, the coupler is designed with $Z_C = 20.97\Omega$ and $k = 0.849$. With these values, R_Z that provides the required cutoff is 1.32.

Next step is to find a R_Z (Fig. 5.12) that provides equal-ripple and required rejection for the chosen k and Z_C. Note that Fig. 5.12 is based on a $Z_C = 28\ \Omega$, so it can only be used as an approximation. The required value for R_{Zstep} is 1.4. By replacing it and R_{Zunif} in (5.35), $R_S = 0.83$ is obtained. A complete summary of the design parameters is shown in Table 5.1.

Coupled lines

l_C	4.33mm
Z_C	20.97 Ω
k	0.849

Loop-line

R_Z	1.4
R_S	0.83
Z_1	29.36 Ω
Z_2	24.37 Ω
θ_1	90^o (4.33 mm)
θ_2	90^o (4.33 mm)

Table 5.1: Design parameters summary

5.8.2 Physical implementation

In order to translate the theoretical design into a real one, some modifications to the model have to be introduced. The structure is divided in two different layers to take advantage of the higher coupling rates of broadside coupled lines. Therefore, the loop-line also has to be split into two sections, one on each layer, and connected by a vertical via located at its middle point. The design is stripline so it can be packaged as described in Chapter 3. With this considerations in place, the design comprises four metal layers: two for the loop structure, and two as ground planes (Fig. 5.16b).

Line widths are determined so their characteristic impedances match the design parameters. The section of loop-line that overlaps to accommodate the via connection is slightly narrower to compensate for the induced coupling (Fig. 5.16a). The design is integrated with the packaging by extending the 50 Ω feed-lines so they end under the external CPW, also matched for 50 Ω (Fig. 5.17a).

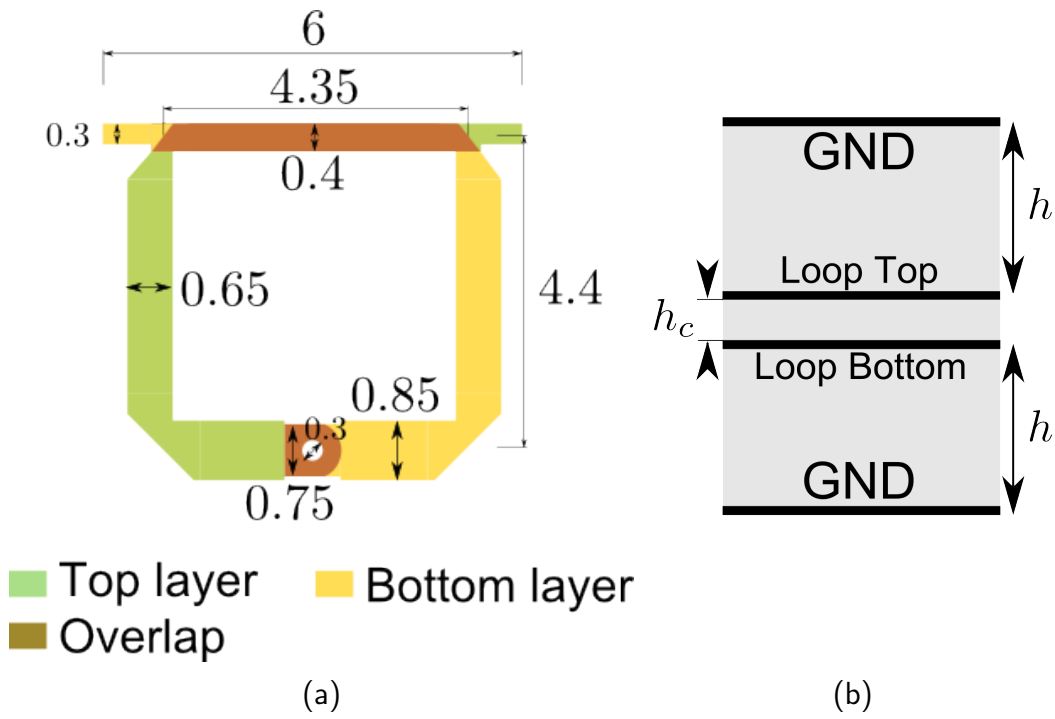


Figure 5.16: Design details (a) Top view (dimensions in mm) (b) Layer distribution ($h_c = 25\mu m$, $h = 0.2mm$)

5.8.3 Fabrication

Fabrication process followed is described in detail in Chapter 2. In this specific case, the via in the middle layer connecting the two parts of the loop structure is drilled and plated before the lamination. Details for the physical layer distribution and mask for the middle layer, containing four samples, are shown in Fig. 5.17. Masks for CPW layer and ground plane are omitted.

5.8.4 Simulation and results

EM simulation results are plotted against the ideal model in Fig. 5.18. Mismatches, mainly in the fourth TZ, are produced by the corners in the loop-line, which are not included in the theoretical model. Spurious coupling and the via transition also contribute to the mismatch.

Measured results are plotted against EM simulation in Fig. 5.19, including the packaging. Even though they show a good correlation, some differences are found. These are due to fabrication tolerances, i.e. substrate thickness and etching. In order to achieve the tight coupling required, the coupled-lines are etched on a 25 μm-thick film (Fig. 5.16b). Its thinness magnifies the error introduced by misalignment

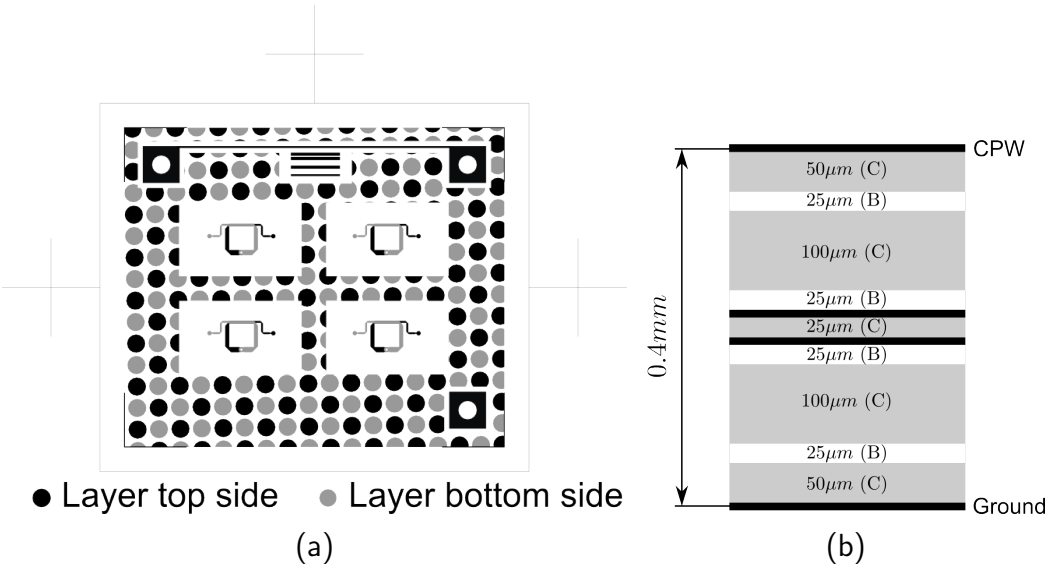


Figure 5.17: Mask and layer distribution for fabrication. (C=Core film, B=Bonding film)

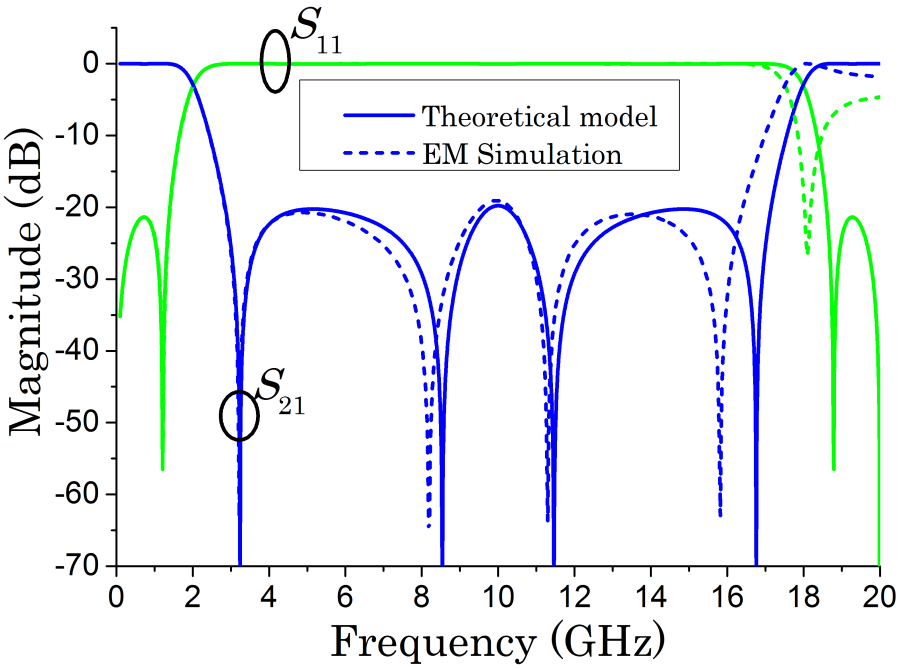


Figure 5.18: Theoretical model vs. EM simulation

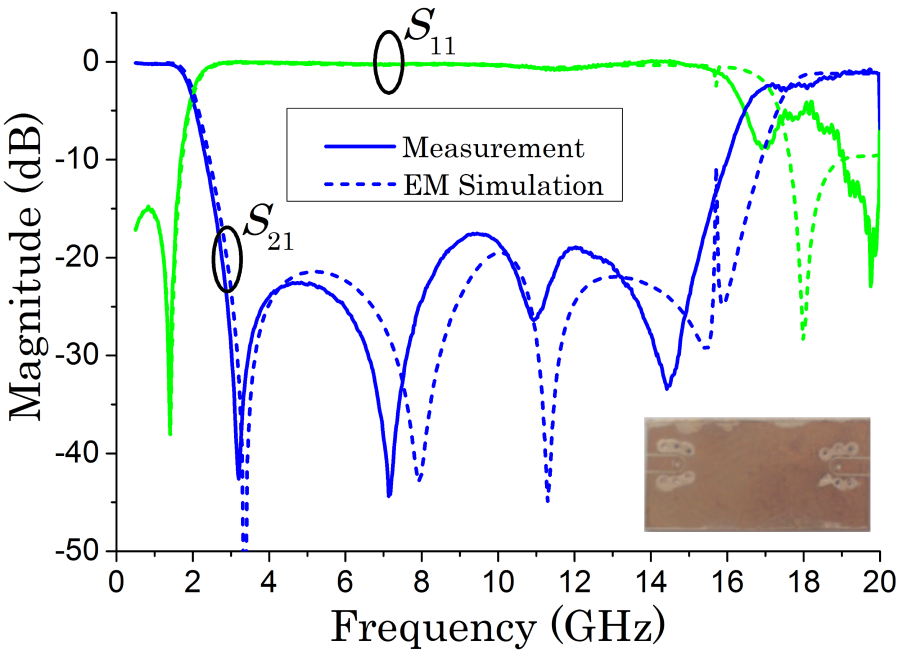


Figure 5.19: Measured results vs. EM simulation, including packaging

f_C	1.97 GHz
Insertion Loss	0.25 dB
Return Loss	13.6 dB
FBW 3dB	157% ($8.37 f_C$)
Roll-off rate	20 dB/GHz
Min. rejection	17 dB
FBW 17dB	139.5%

Table 5.2: Measured results summary

and over-compression, explaining the mismatch in the results. A summary of the measured properties is shown in Table 5.2.

5.9 High-rejection LPF with 3 GHz cutoff frequency

In this design we aim at designing a low-pass filter with improved rejection in order to validate the discussion from Sections 5.6 and 5.7. Initial requirements for the low pass filter are:

- Cutoff frequency: 3 GHz
- Stopband up to 8 f_C, equivalent to 155% fractional bandwidth (FBW)

Coupled lines

l_C	3.21 mm
Z_C	28.14 Ω
k	0.734

Loop-line

R_Z	1.44
R_S	1.26
Z_1	40.52 Ω
Z_2	51.05 Ω
θ_1	90^o (3.21 mm)
θ_2	90^o (3.21 mm)

Table 5.3: Basic cell design parameters summary

- Equal ripple with, at least, 40 dB rejection

Such requirements cannot be fulfilled by a single loop structure. Instead, two of them with identical parameters are cascaded. As cascading two identical filters doubles the rejection level, each of these filters need to be designed for a 20 dB rejection, while keeping the rest of requirements. In the following sections design stages are described, starting from a basic design, then reducing its footprint, and finally cascading.

5.9.1 Basic cell parameters design

Initial design is based on the procedure described in Section 5.5. For a 155% FBW, the required $\theta_{3dB} = 20^o$, resulting in $l_C = 3.21$ mm. Coupled lines are designed with $Z_C = 28.14$ and $k = 0.734$, and the R_Z that provides the required cutoff (Fig. 5.8) is 1.56. Furthermore, values for obtaining a 20 dB equal-ripple in the stopband are $R_Z = 1.44$ and $R_S = 1.27$ (Fig. 5.12). Simulated results for this configuration are plotted in Figure 5.20.

5.9.2 Footprint reduction

Based on optimization, the new values for the impedance ratios are $R_Z = 1.26$ and $R_S = 1.22$, and $\theta_{C1} = 10^o$. Thus, the length of the coupled lines is increased by 22%, being the new $l_C = 3.92$ mm. With these values, a similar response with the same f_C is obtained, as well as same rejection levels, with slightly reduced stopband width (Fig. 5.20). These modifications lead to a 25% footprint reduction.

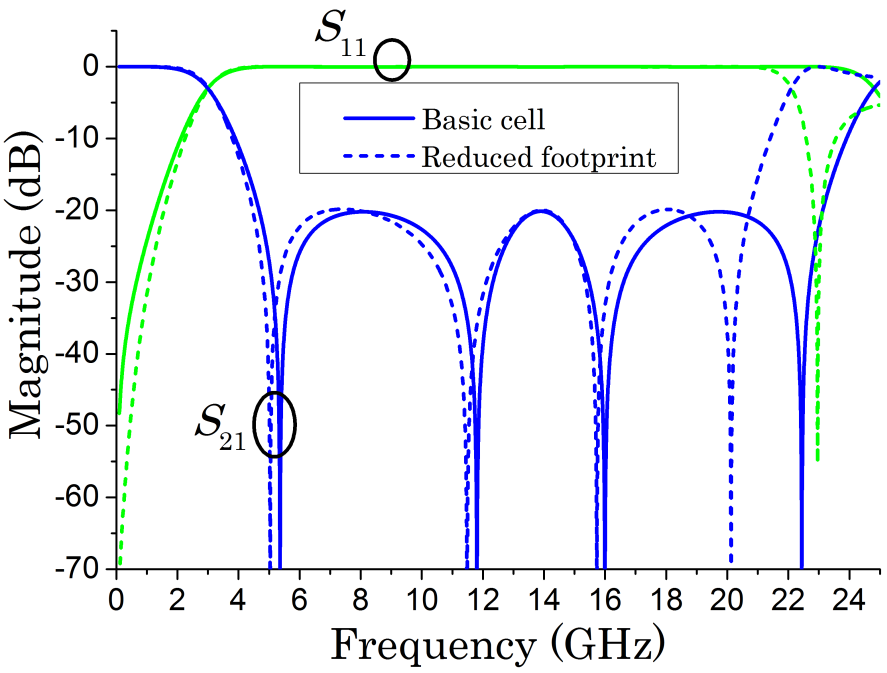


Figure 5.20: Basic cell and reduced footprint simulation

Coupled lines

l_C	3.92 mm
Z_C	28.14 Ω
k	0.734
θ_{C1}	10^o (0.43 mm)
θ_{C3}	10^o (0.43 mm)

Loop-line

R_Z	1.26
R_S	1.22
Z_1	35.46 Ω
Z_2	43.26 Ω
θ_1	45^o (1.96 mm)
θ_2	90^o (3.92 mm)

Table 5.4: Reduced footprint design parameters summary

5.9.3 Cascading

The basic unit was designed for a 3 GHz cutoff frequency. This will need to be adjusted for a -1.5 dB, 3 GHz so the cascaded filter results in a 3 GHz at -3 dB. Therefore, l_C needs to be adjusted to 3.42 mm.

As discussed in previous sections, the two filtering units are connected by a uniform transmission line. The length and impedance of this line is designed to match Z_{in} at the first TZ. At this frequency, $Z_{in}(\theta_{TZ1}) = -j22.4\Omega$. By fixing $Z_J = 50\Omega$ and using (5.24), the matching value of θ_J is 54^o.

In order to match the rest of the Z_{in} singularities with the remaining three TZs, two parameters are optimized: the width of the via patch, and its shifting from the center of the line section parallel to the coupled lines (Fig. 5.21). Note that shifting

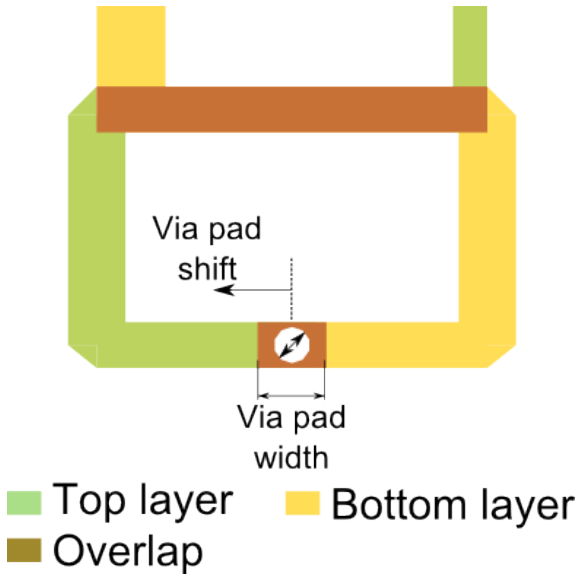


Figure 5.21: Optimization parameters

from the center towards left or right is equivalent, since the structure is symmetrical. Modifications to these parameters have no effect on the first TZ. Their impact on the last three TZ is shown in Figures 5.22 and 5.23).

A summary with all the design parameters after optimization is gathered in Table 5.5. Feed lines are designed to improve the return loss, with an impedance of 32Ω and a length of 50^o.

Coupled lines

l_C	3.4 mm
Z_C	28.14 Ω
k	0.734
θ_{C1}	$10^o(0.4mm)$
θ_{C3}	$6^o(0.2mm)$

Loop-line

R_Z	1.26
R_S	1.2
Z_1	35.46 Ω
Z_2	42.55 Ω
θ_1	$53^o(2mm)$
θ_2	$90^o(3.4mm)$
Via pad width	0.75 mm
Via pad shift	1.05 mm

Cascading line

Z_J	50 Ω
θ_J	$54^o(2.05mm)$

Table 5.5: Final design parameters summary

5.9.4 Physical implementation

As in the previous design, the filter is physically implemented in four metal layers: two for the filter, and two for the ground planes, so it can be packaged using the technique covered in Chapter 3. In order to avoid excessive intra-cell coupling, two

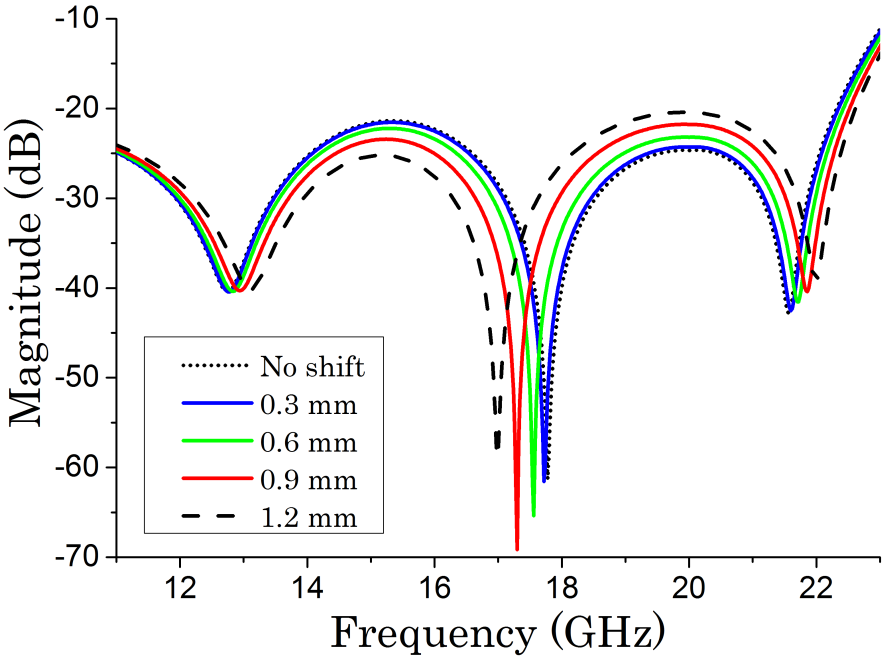


Figure 5.22: Via-pad shift effect on the last three TZs (simulated results)

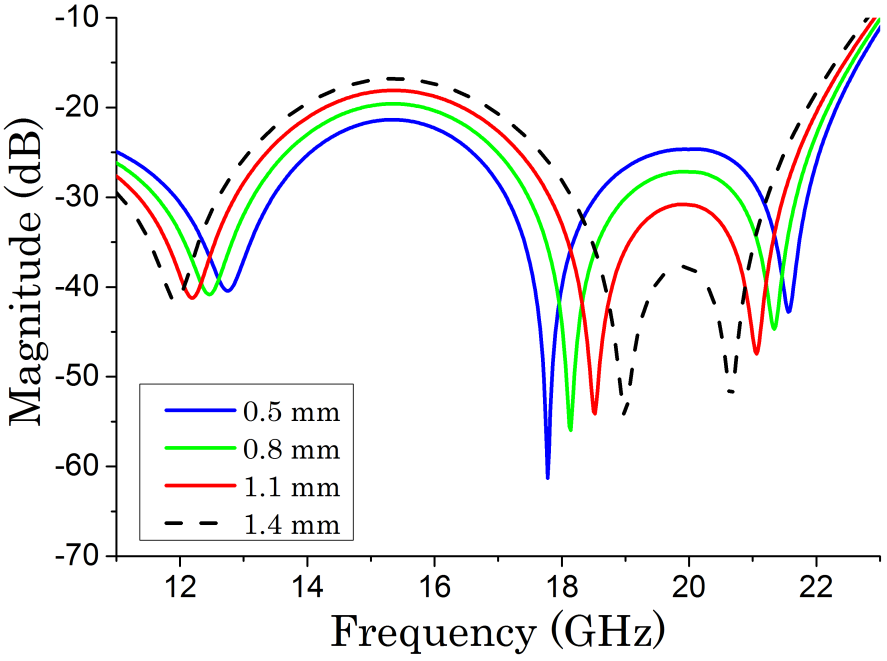


Figure 5.23: Via-pad width effect on the last three TZs (simulated results)

vias are included connecting both ground planes, also contributing to maintaining an even potential between them. The complete layout is included in Figure 5.24.

5.9.5 Fabrication

Fabrication process followed is described in detail in Chapter 2. The via in the middle layer connecting the two parts of the loop structure is drilled and plated before the lamination. Details for the physical layer distribution and mask for the middle layer, containing three samples, are shown in Fig. 5.25. Masks for CPW layer and ground plane are omitted (see Chapter 3 for details). The fabricated filter has a small footprint (16.4×6.6 mm^2, packaging included) and very low profile (0.45 mm), as well as very light weight (0.162 gr.).

5.9.6 Simulation and results

Full EM simulation for the cascaded design is plotted in Fig. 5.26, including the simulation for the optimized basic unit. It can be appreciated how the Z_{in} singularities for the basic unit are matched with the TZs. In both cases simulations correspond to designs including packaging.

Regarding the simulation, there is a noticeable mismatch in the location of the second TZ, and a slight mismatch in the other three. This is mainly produced by the induced coupling between the two basic units. Even though, Z_{in} is not perfectly matched due to the mutual coupling, expected resonances are effectively attenuated without compromising the equal-ripple response.

Furthermore, overall results show a good agreement with the simulations, presenting a low insertion loss and group delay. A summary of the merit figures of the filter is shown in Table 5.6.

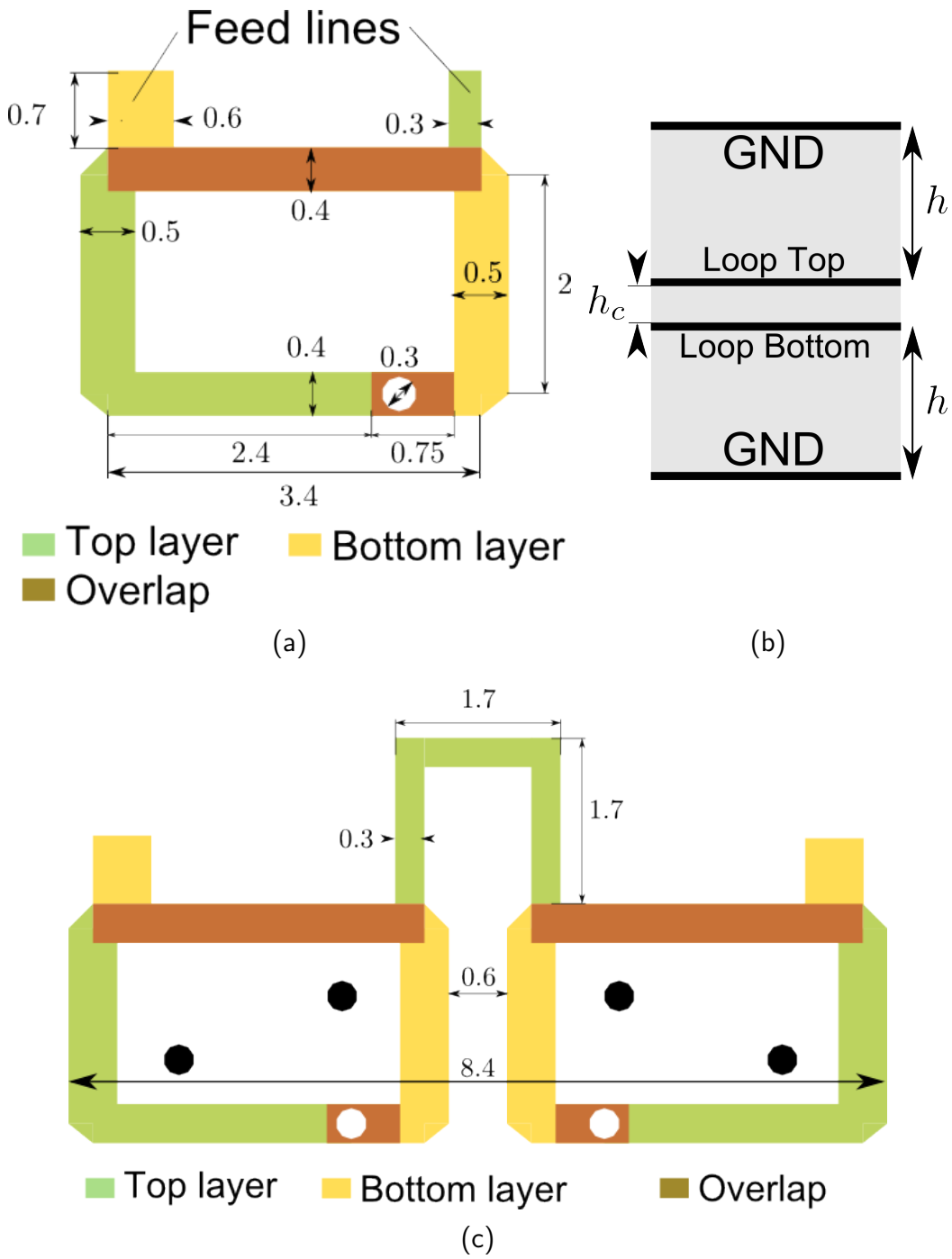


Figure 5.24: Final design details (a) Optimized unit (dimensions in mm) (b) Layer distribution ($h_c = 50\mu m$, $h = 0.2mm$) (c) Cascaded design (dimensions in mm). Ground vias in black.

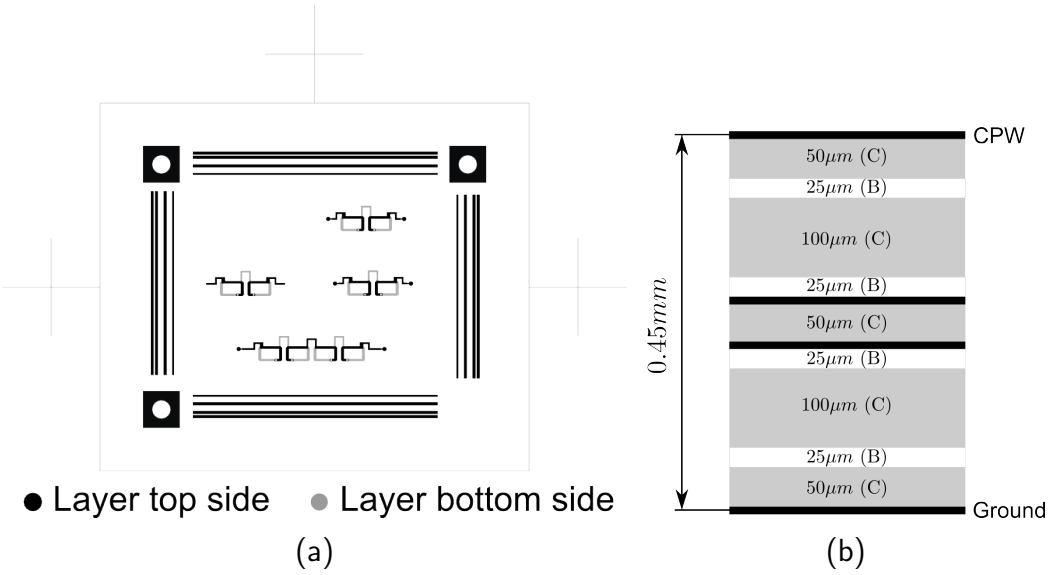


Figure 5.25: Mask and layer distribution for fabrication. (C=Core film, B=Bonding film)

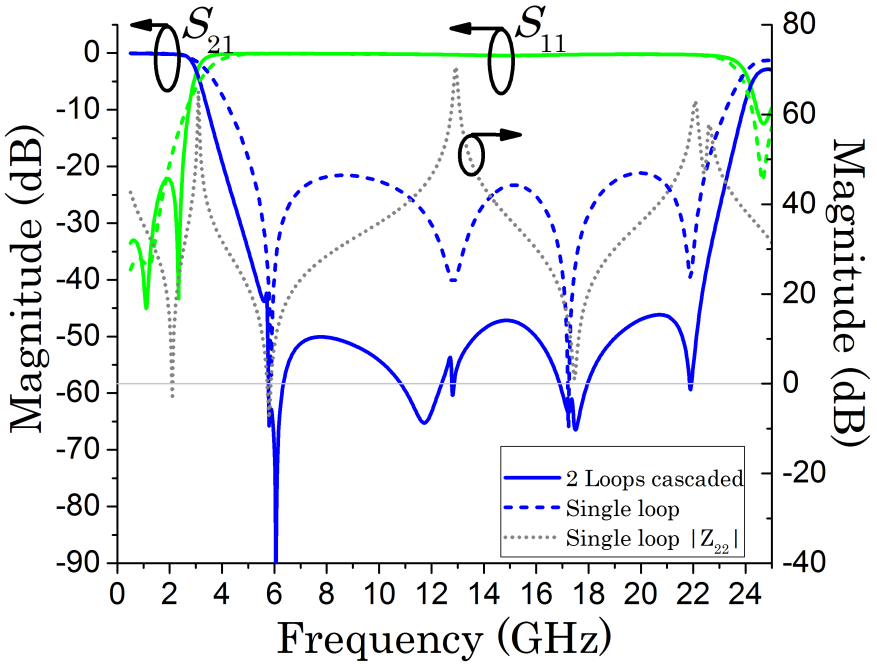
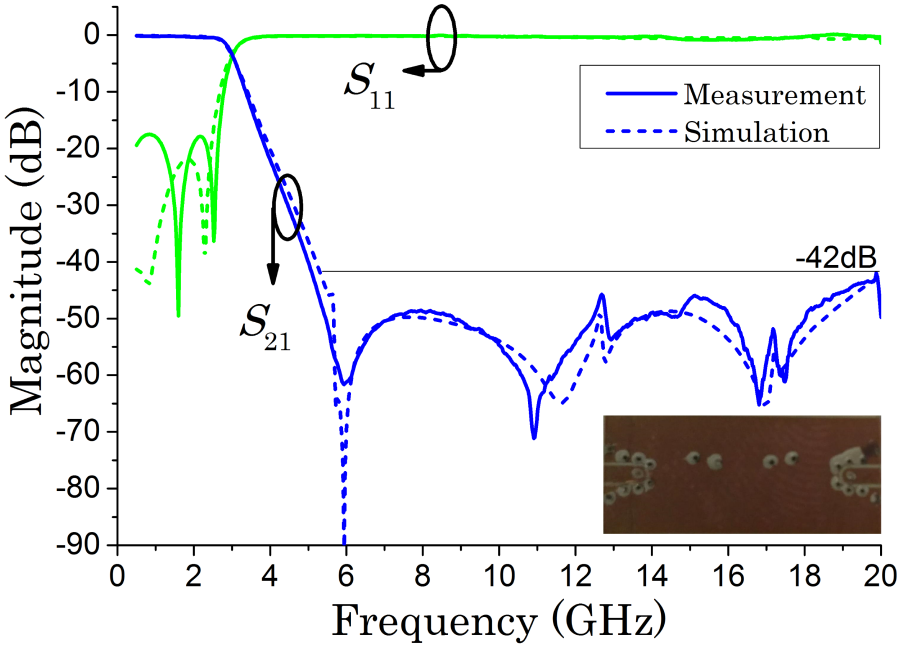


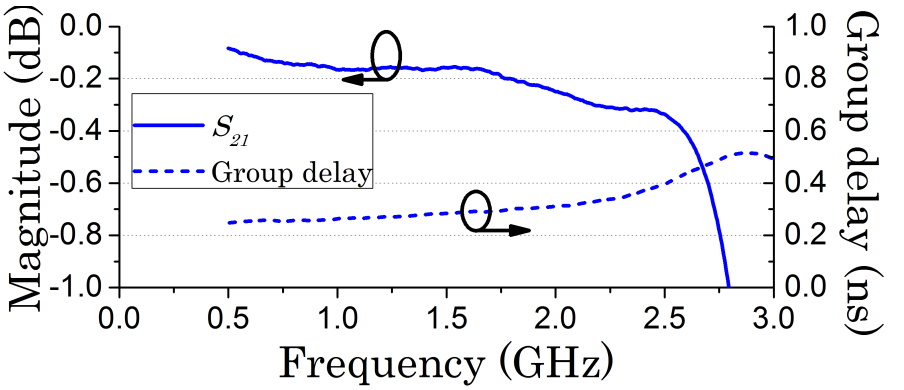
Figure 5.26: Basic cell vs. cascaded. Scattering parameters, simulated results

f_C	3 GHz
Insertion Loss	0.4 dB
Return Loss	17.6 dB
FBW 3dB	157% ($8.37 f_C$)
Roll-off rate	18.48 dB/GHz
Min. rejection	43 dB
FBW 43dB	139.5%

Table 5.6: Measured results summary



(a)



(b)

Figure 5.27: Measured results vs. Simulation (including packaging) (a) Wideband response. Picture of the fabricated prototype (b) Insertion loss and group delay

5.10 Very high-rejection LPF with 3 GHz cutoff frequency

In order to further demonstrate the improvement in the rejection of the stopband by cascading, a new design is proposed. The aim of this design is to test how successive cascading would affect the insertion loss and how much improvement could be achieved in the stopband.

5.10.1 Design

The filter is based on the previous two-cell design, maintaining the same cell design but cascading four units in this case. In other words, cascading together two double-cell filters. The only element optimized for this design is the interconnection line between the two pairs of cells, with a length of 50^o (1.9 mm) and a characteristic impedance of 50 Ω (Fig. 5.10.1).

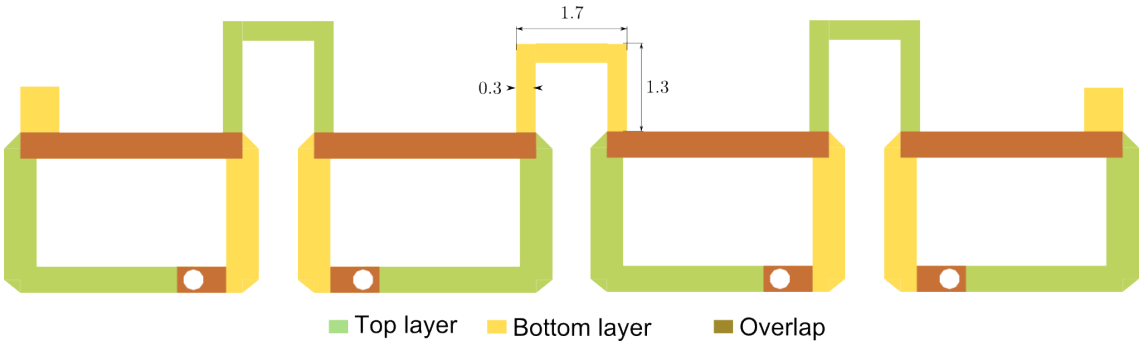


Figure 5.28: 4 basic cells cascaded design. Dimensions in mm. For the rest of dimensions see Fig. 5.24

5.10.2 Fabrication

The filter is fabricated along with the two-cell cascaded design, see Section 5.9.5. Mask for this design is shown at the bottom of Fig. 5.25a. The size of the fabricated sample is measured at 27.8×5.5 mm^2.

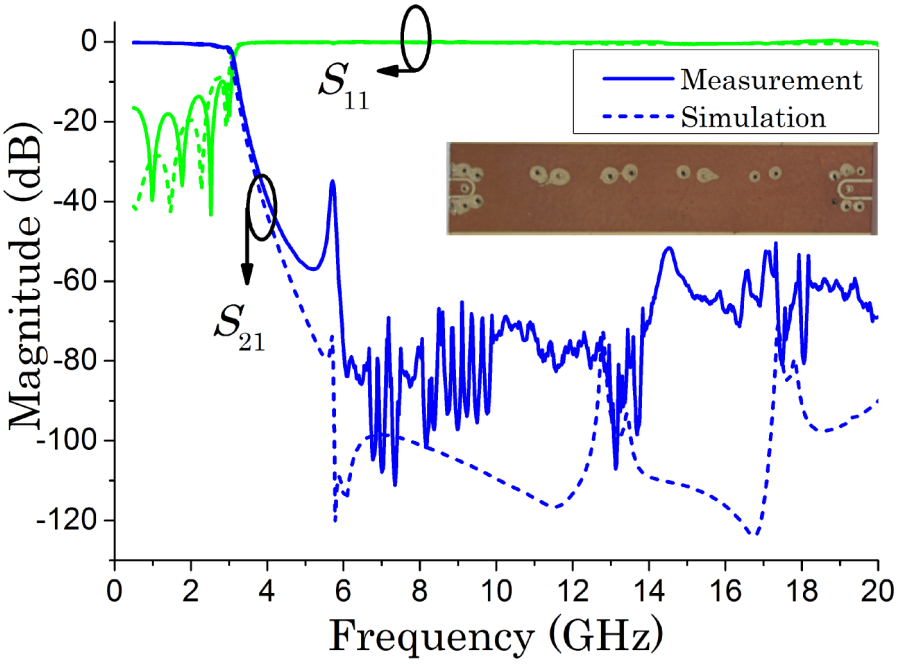


Figure 5.29: 4 basic cells cascaded design results

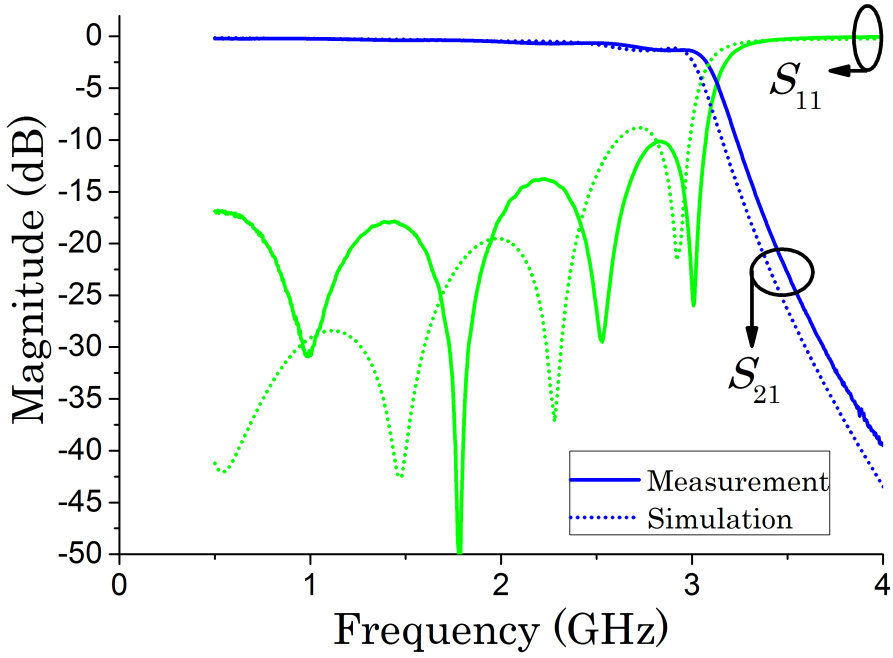
5.10.3 Simulation and results

EM simulations against measured results are shown in Fig. 5.29. According to the simulations, the expected levels of rejection are in the region of -90 dB. However, measurements show a maximum rejection of 60-70 dB, owing to the noise floor of the VNA used for measuring. Also noticeable is the resonance around 6 GHz, corresponding to the mismatch between the first TZ and the input impedance (see Section 5.7).

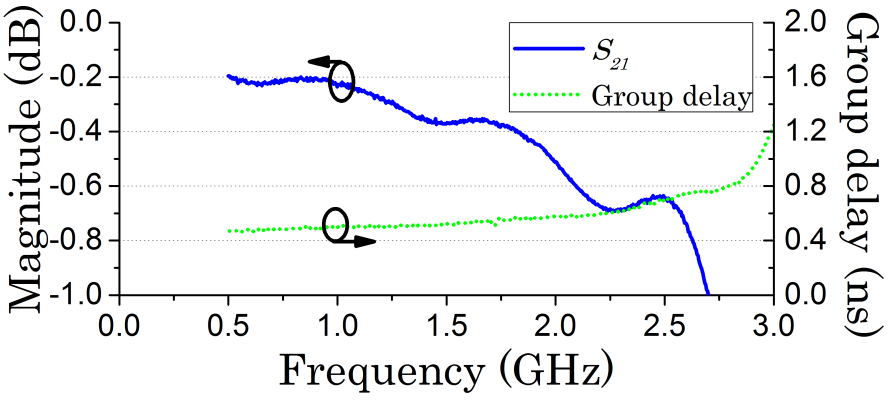
Regarding the passband, it shows four poles, instead of two, as the order of the filter has been increased (Fig. 5.30a). However, the return loss is not uniform, suggesting the filter would need further optimization. As expected, insertion loss and group delay are higher than those of the two-cells version since the signal has to travel a path twice as long, increasing the ohmic losses. A complete summary of the measured filter's properties is shown in Table 5.7.

f_C	3 GHz
Insertion Loss	0.7 dB
Return Loss	10 dB
FBW 3dB	157% ($8.37 f_C$)
Roll-off rate	33.33 dB/GHz
Min. rejection	50 dB
FBW 50dB	126%

Table 5.7: Measured results summary



(a)



(b)

Figure 5.30: Measured results vs. Simulation (including packaging) (a) Wideband response. Picture of the fabricated prototype (b) Insertion loss and group delay

5.11 Conclusions and future work

Along this chapter a filtering structure based on destructive interference has been analysed. Starting from a basic design, subsequent modifications to the feedback impedance have been introduced and its advantages explained, also including approaches for footprint reduction.

It has been demonstrated how introducing a stepped-impedance loop-line enables a much higher flexibility in the design, compared to its uniform loop-line counterpart, where rejection levels for a flat stopband were mainly limited by the design of the coupled lines. Moreover, the loop-line's impedance ratio can compensate for their coupling coefficient, by merely changing the width of the line, rather than modifying the gap or the offset between the coupled lines.

Furthermore, matters involving interconnection of loop-line filters has been discussed, proposing a method for cancelling spurious resonances by matching them with the transmission zeroes.

In order to demonstrate the theory, three different filters have been designed and fabricated, covering a single-unit filter, two cascaded filters, and four cascaded filters. Designs have been carried following the proposed method and measured results are in good agreement with the simulations. For reference, performance parameters of these filters are included in Table 5.8, along with some other relevant works found in the open literature.

The design has been proved to adapt successfully for the available fabrication techniques and equipment, even though higher resolution manufacturing could enhance the results. It is also particularly suitable for low-profile stripline configurations, where relatively low values for characteristic impedances are obtained. Furthermore, these filters are better suited for cutoff frequencies in the range of 2-6 GHz. Higher frequencies may be achieved with improved miniaturization fabrication techniques, even though the roll-off performance degrades at higher frequencies.

As future work, it would be interesting to try out this type of designs in substrates with higher dielectric constant, in order to test how much the footprint can be reduced and whether it would suit available fabrication techniques with other materials.

Table 5.8: Performance comparison among published filters

Ref.	f_c	IL (dB) / RL (dB)	Roll-off rate (dB/GHz)	Stopband RJL (dB) / FBW (%)	NCS (λ_g^2)	# Casc. Cells
[2]	2.5	0.45 / 14	24.3	20 / 114.7	0.290 x 0.070	2
[4]	0.5	0.5 / 16.3	95	20 / 140	0.104 x 0.214	1
[5]	3	N/A / 12	42.7	25 / 150	0.310 x 0.240	4
[6]	1.76	0.39 / 14	94.9	23 / 160	0.104 x 0.123	1
[7]	3.12	0.33 / 11.54	30.35	20 / 135.1	0.290 x 0.110	1
[8]	3	0.03 / 20	58.6	25 / 143	0.220 x 0.110	1
[9]	1	0.4 / N/A	21.8	15 / 165.5	0.111 x 0.091	1
[10]	1	0.4 / 20	63	20 / 166.1	0.107 x 0.083	1
[15]	1.26	0.8 / 9	217	20 / 168.5	0.120 x 0.290	1
Section 5.8	2	0.25 / 13.7	20	17 / 139.5	0.070 x 0.070*	1
Section 5.9	3	0.4 / 17.6	18.48	43 / 126	0.161 x 0.070*	2
Section 5.10	3	0.7 / 10	33.33	50 / 126	0.306 x 0.070*	4

f_c = Cutoff frequency (3 dB); IL = Insertion Loss; RL = Return Loss;
RJL = Rejection level; FBW = Fractional bandwidth;
NCS = Normalized circuit size; λ_g = Guided wavelength at f_c
(*) Packaging not included

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Chapter 6

Conclusions and future work

6.1 Conclusions

This thesis has covered the development of miniature, self-packaged, planar filters using liquid crystal polymer (LCP) as a microwave substrate, as well as packaging material. This development required, in first place, a comprehensive analysis and review of the available fabrication techniques, that carried into the design of a packaging solution also based on LCP techniques. The packaging was then applied to two different types of filters in order to validate its performance.

In Chapter 2 the fabrication process was covered. Starting from the available in-house fabrication process, the weak points were highlighted, mainly the lamination process and the production of narrow, blind via holes. Main contribution from this chapter is successful implementation of a fabrication process where every LCP layer is processed independently, and via holes drilled before the lamination process. This new process represents a big improvement from the original process by increasing the reliability of via connections. Furthermore, the layer-by-layer process allows for quality control before the lamination, and layers not passing the quality test can be replaced without discarding the whole circuit. This is particularly interesting for industrial processes.

Chapter 3 is aimed at developing a packaging solution for planar filters that could be integrated with current design and fabrication processes. Typically an external box was added to planar filters once they were fabricated in order to protect them from the environment, usually made of aluminium. This type of solution significantly

increases the weight of the final device, as well as its volume. The proposed packaging system uses the same material as the one used for the filter, eliminating the need for foreign materials in the final solution. Along the chapter, three different designs are investigated progressively. Early stages of this research were published in [1,2]. The final solution provides low insertion loss, only increasing size and weight minimally. Additionally, the design comprises a coplanar waveguide (CPW) interface that allows for easy interconnection with a host PCB board.

Work carried in Chapters 2 and 3 is mainly concerned with the improvement of fabrication techniques. Both were developed in parallel and their conclusions and findings applied to the research on chapters 4 and 5, which are focused on the design of novel, multilayer filters.

In Chapter 4 a new type of structure for implementing dual-band filters is presented. The structure is based on a multi-mode resonator, FMSIR, capable of providing increased separation between the desired resonant modes and the unwanted ones. This translates into filters with increased out-of-band rejection. The proposed structure also provide independent control over the passbands so they can be designed with different fractional bandwidth or return loss. The design also takes advantage of multilayer techniques, reducing the footprint significantly when compared to filters of similar performance in the open literature. The developed filter integrates with the proposed packaging structure. Two different filters are designed and fabricated based on this approach, providing excellent results. A summary of the work carried in this chapter is published in [3].

A different type of filter is introduced in Chapter 5, a lowpass filter in this case. The aim of this design is to implement a lowpass filter with wide, deep rejection and very low insertion loss, while requirements for a sharp transition from passband to stopband are relaxed. The structure used is based on the principle of destructive interference and is formed by a pair of broadside coupled lines connected by a feedback transmission line. Different configurations for the feedback impedance are investigated and the modifications introduced to the filter response analysed. Furthermore, in order to increase the rejection levels of the filter, cascading of two and four loop-structures is analysed, obtaining rejections better than 60 dB for a wide frequency range. Successful cascading of filters required a method to cancel spurious resonances with the available transmission zeroes. In order to validate the

theory discussed in this chapter, three different filters are fabricated using the self-packaging technique previously covered. Results for the three configurations are in good agreement with the simulations. Part of this work has been published in [4].

In general, the work carried in this thesis has shown how multilayer LCP techniques can be applied to fabricate self-packaged filters, while maintaining the manufacturing costs to a minimum, and may represent an alternative to better established technologies like LTCC.

6.2 Future work

Some of the topics covered in this thesis open possibilities for future work.

- In chapter 2, the two types of LCP used have melting temperatures that are fairly close to each other, originating some fabrication issues. As the substrate provided recently released a new product where this temperature difference is increased, it would be interesting to evaluate the improvement in the fabrication results with these new materials.
- Also regarding fabrication, increased number of metal layers in a circuit has not been sufficiently tested. Increasing the amount of layers may lead to footprint reduction in future designs.
- The packaging solution proposed in Chapter 3 relies on the application of a conductive paste on the side walls in order to provide full electromagnetic isolation. However, an accurate measurement of how external radiation would affect the performance of the filter has not been performed.
- Lowpass filter proposed in Chapter 5 shows good a very good performance in terms of rejection when cascading two units, at the cost of increased footprint. During the development of this filter it was found that coupling between two cascaded units could potentially split the transmission zeroes, generating additional ones. This could improve the response of the filter, apart from making easier the matching between two cascaded units. Furthermore, this coupling could be investigated when the loops are placed on top of each other, leading to a significant footprint reduction.

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